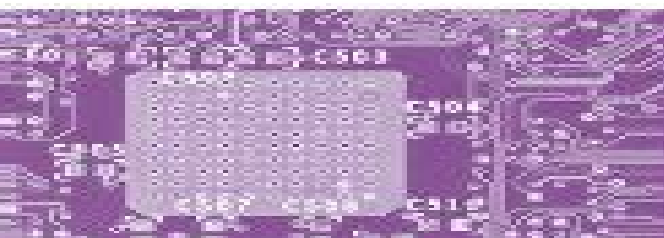




ESD

ANALOG CIRCUITS AND DESIGN

STEVEN H. VOLDMAN



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Esd Design For Analog Circuits

Steven H. Voldman



Esd Design For Analog Circuits:

ESD Steven H. Voldman, 2014-07-30 A comprehensive and in depth review of analog circuit layout schematic architecture device power network and ESD design This book will provide a balanced overview of analog circuit design layout analog circuit schematic development architecture of chips and ESD design It will start at an introductory level and will bring the reader right up to the state of the art Two critical design aspects for analog and power integrated circuits are combined The first design aspect covers analog circuit design techniques to achieve the desired circuit performance The second and main aspect presents the additional challenges associated with the design of adequate and effective ESD protection elements and schemes A comprehensive list of practical application examples is used to demonstrate the successful combination of both techniques and any potential design trade offs Chapter One looks at analog design discipline including layout and analog matching and analog layout design practices Chapter Two discusses analog design with circuits examining single transistor amplifiers multi transistor amplifiers active loads and more The third chapter covers analog design layout also MOSFET layout before Chapters Four and Five discuss analog design synthesis The next chapters introduce the reader to analog digital mixed signal design synthesis analog signal pin ESD networks and analog ESD power clamps Chapter Nine the last chapter covers ESD design in analog applications Clearly describes analog design fundamentals circuit fundamentals as well as outlining the various ESD implications Covers a large breadth of subjects and technologies such as CMOS LDMOS BCD SOI and thick body SOI Establishes an ESD analog design discipline that distinguishes itself from the alternative ESD digital design focus Focuses on circuit and circuit design applications Assessable with the artwork and tutorial style of the ESD book series PowerPoint slides are available for university faculty members Even in the world of digital circuits analog and power circuits are two very important but under addressed topics especially from the ESD aspect Dr Voldman's new book will serve as an essential and practical guide to the greater IC community With high practical and academic values this book is a bible for professionals graduate students device and circuit designers for investigating the physics of ESD and for product designs and testing

ESD Design for Analog Circuits Vladislav A. Vashchenko, Andrei Shibkov, 2010-07-27 This Book and Simulation Software Bundle Project Dear Reader this book project brings to you a unique study tool for ESD protection solutions used in analog integrated circuit IC design Quick start learning is combined with in depth understanding for the whole spectrum of cross disciplinary knowledge required to excel in the ESD field The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies The book project provides two different options for learning the material The printed material can be studied as any regular technical textbook At the same time another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise The book is bundled with simplified trial

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The ESD Handbook Steven H. Voldman, 2021-04-12 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems

ESD Steven H. Voldman, 2011-04-04 Electrostatic discharge ESD continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I/O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I/O guard rings ESD guard rings I/O to I/O and I/O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies discussed including CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS and smart power practical methods for the

understanding of ESD circuit power distribution ground rule development internal bus distribution current path analysis quality metrics ESD Design and Synthesis is a continuation of the author's series of books on ESD protection It is an essential reference for ESD circuit and semiconductor engineers design synthesis team leaders layout design characterisation floorplanning test and reliability engineers technicians and groundrule and test site developers in the manufacturing and design of semiconductor chips It is also useful for graduate and undergraduate students in electrical engineering semiconductor sciences and manufacturing sciences and on courses involving the design of ESD devices chips and systems This book offers a useful insight into the issues that confront modern technology as we enter the nano electronic era **ESD**

Basics Steven H. Voldman, 2012-10-22 Electrostatic discharge ESD continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book introduces the fundamentals of ESD electrical overstress EOS electromagnetic interference EMI electromagnetic compatibility EMC and latchup as well as provides a coherent overview of the semiconductor manufacturing environment and the final system assembly It provides an illuminating look into the integration of ESD protection networks followed by examples in specific technologies circuits and chips The text is unique in covering semiconductor chip manufacturing issues ESD semiconductor chip design and system problems confronted today as well as the future of ESD phenomena and nano technology Look inside for extensive coverage on The fundamentals of electrostatics triboelectric charging and how they relate to present day manufacturing environments of micro electronics to nano technology Semiconductor manufacturing handling and auditing processing to avoid ESD failures ESD EOS EMI EMC and latchup semiconductor component and system level testing to demonstrate product resilience from human body model HBM transmission line pulse TLP charged device model CDM human metal model HMM cable discharge events CDE to system level IEC 61000 4 2 tests ESD on chip design and process manufacturing practices and solutions to improve ESD semiconductor chip solutions also practical off chip ESD protection and system level solutions to provide more robust systems System level concerns in servers laptops disk drives cell phones digital cameras hand held devices automobiles and space applications Examples of ESD design for state of the art technologies including CMOS BiCMOS SOI bipolar technology high voltage CMOS HVCMOS RF CMOS smart power magnetic recording technology micro machines MEMs to nano structures ESD Basics From Semiconductor Manufacturing to Product Use complements the author's series of books on ESD protection For those new to the field it is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic Era **ESD**

Steven H. Voldman, 2006-02-03 The scaling of semiconductor devices from sub micron to nanometer dimensions is driving the need for understanding the design of electrostatic discharge ESD circuits and the response of these integrated circuits IC to ESD phenomena ESD Circuits and Devices provides a clear insight into the layout and design of circuitry for protection against electrical overstress EOS and ESD With an emphasis on examples this text explains ESD buffering ballasting current

distribution design segmentation feedback coupling and de coupling ESD design methods outlines the fundamental analytical models and experimental results for the ESD design of MOSFETs and diode semiconductor device elements with a focus on CMOS silicon on insulator SOI and Silicon Germanium SiGe technology focuses on the ESD design optimization integration and synthesis of these elements and concepts into ESD networks as well as applying within the off chip driver networks and on chip receivers and highlights state of the art ESD input circuits as well as ESD power clamps networks Continuing the author's series of books on ESD this book will be an invaluable reference for the professional semiconductor chip and system ESD engineer Semiconductor device and process development quality reliability and failure analysis engineers will also find it an essential tool In addition both senior undergraduate and graduate students in microelectronics and IC design will find its numerous examples useful

Electrostatic Discharge Steven Voldman, 2019-10-02 As we enter the nanoelectronics era electrostatic discharge ESD phenomena is an important issue for everything from micro electronics to nanostructures This book provides insight into the operation and design of micro gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies electrical breakdown in micro gaps nanogenerators from ESD and theoretical prediction and optimization of triboelectric nanogenerators The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design

Electrostatic Discharge Protection Juin J. Liou, 2017-12-19 Electrostatic discharge ESD is one of the most prevalent threats to electronic components In an ESD event a finite amount of charge is transferred from one object i e human body to another i e microchip This process can result in a very high current passing through the microchip within a very short period of time Thus more than 35 percent of single event chip damages can be attributed to ESD events and designing ESD structures to protect integrated circuits against the ESD stresses is a high priority in the semiconductor industry Electrostatic Discharge Protection Advances and Applications delivers timely coverage of component and system level ESD protection for semiconductor devices and integrated circuits Bringing together contributions from internationally respected researchers and engineers with expertise in ESD design optimization modeling simulation and characterization this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection Amply illustrated with tables figures and case studies the text Instills a deeper understanding of ESD events and ESD protection design principles Examines vital processes including Si CMOS Si BCD Si SOI and GaN technologies Addresses important aspects pertinent to the modeling and simulation of ESD protection solutions Electrostatic Discharge Protection Advances and Applications provides a single source for cutting edge information vital to the research and development of effective robust ESD protection solutions for semiconductor devices and integrated circuits

System Level ESD Protection Vladislav Vashchenko, Mirko Scholz, 2014-03-21 This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge ESD protection It is an invaluable reference for anyone developing systems on chip SoC and systems on package SoP integrated with system level ESD protection The book

focuses on both the design of semiconductor integrated circuit IC components with embedded on chip system level protection and IC system co design The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits thereby reducing or completely eliminating the need for additional discrete components on the printed circuit board PCB and meeting system level ESD requirements The authors take a systematic approach based on IC system ESD protection co design A detailed description of the available IC level ESD testing methods is provided together with a discussion of the correlation between IC level and system level ESD testing methods The IC level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing The overall methodology for IC system ESD co design is presented as a step by step procedure that involves both ESD testing and numerical simulations

Handbook of Research on Developments in E-Health and Telemedicine: Technological and Social Perspectives Cruz-Cunha, Maria Manuela,Tavares, Antonio J.,Simoes, Ricardo,2009-12-31 This book provide a comprehensive coverage of the latest and most relevant knowledge developments solutions and practical applications related to e Health this new field of knowledge able to transform the way we live and deliver services both from the technological and social perspectives Provided by publisher

Edn Designers Guide to Electromagnetic Compatibility Daryl D Gerke,Bill Kimmel,2002-08-01 In 1996 enforcement of the mandatory European Union EMI EMC electromagnetic interference and compatibility began Before that time many designers were just beginning to worry about EMI problems Now 8 years later the same old EMI problems are still with us and some new ones have emerged as well Anyone selling components or equipment of any sort in Europe and therefore the world for most globally based companies requires compliance with the EMC directive There is no alternative The information in this book enables faster cheaper compliance

ESD Testing Steven H. Voldman,2016-10-14 With the evolution of semiconductor technology and global diversification of the semiconductor business testing of semiconductor devices to systems for electrostatic discharge ESD and electrical overstress EOS has increased in importance ESD Testing From Components to Systems updates the reader in the new tests test models and techniques in the characterization of semiconductor components for ESD EOS and latchup Key features Provides understanding and knowledge of ESD models and specifications including human body model HBM machine model MM charged device model CDM charged board model CBM cable discharge events CDE human metal model HMM IEC 61000 4 2 and IEC 61000 4 5 Discusses new testing methodologies such as transmission line pulse TLP to very fast transmission line pulse VF TLP and future methods of long pulse TLP to ultra fast TLP UF TLP Describes both conventional testing and new testing techniques for both chip and system level evaluation Addresses EOS testing electromagnetic compatibility EMC scanning to current reconstruction methods Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing ESD Testing From Components to Systems is part of the authors series of books on electrostatic discharge ESD protection this book will be an invaluable reference for the professional semiconductor chip

and system level ESD and EOS test engineer Semiconductor device and process development circuit designers quality reliability and failure analysis engineers will also find it an essential reference In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics semiconductor testing and experimental work

Electron Paramagnetic Resonance Studies of Point Defects in AlGa_{1-x}N and SiC Xuan Thang Trinh, 2015-05-12

Point defects in semiconductor materials are known to have important influence on the performance of electronic devices For defect control knowledge on the model of defects and their properties is required Information on defects such as the symmetry and the localization of spins is essential for identification of defects and understanding their electronic structure Such information can be obtained from Electron Paramagnetic Resonance EPR In many cases the energy levels of defects can be determined from photoexcitation EPR photo EPR or temperature dependence of the EPR signal The thesis contains six papers focusing on the identification and electronic structure investigation of defects and impurities in Al_xGa_{1-x}N and silicon carbide SiC using EPR in combination with other electrical characterizations and density functional theory calculations The two first papers concern EPR studies of silicon Si in AlGa_{1-x}N alloys Due to its direct and wide band gap which can be tailored from 3.4 eV for GaN to 6.2 eV for AlN high Al content wurtzite Al_xGa_{1-x}N has been considered as a promising material for fabrication of compact high efficiency and non toxic deep ultraviolet light emitting diodes LEDs and laser diodes LDs for replacing low efficiency and toxic mercury lamps in water air purification and sterilization Si is commonly used for n type doping in AlGa_{1-x}N and AlN but the conductivity of Si doped Al_xGa_{1-x}N was often reported to drop abruptly at high Al content and the reason was often speculated to be due to either carrier compensation by other deep levels or Si itself when it transforms from a shallow donor to a DX or negative U center which acts as an acceptor In paper 1 we showed that Si already forms a stable DX center in Al_xGa_{1-x}N with $x = 0.77$ However with the Fermi level locating only 3 meV below the neutral charge state E_d Si still behaves as a shallow donor Negligible carrier compensation by oxygen O in Al_{0.77}Ga_{0.23}N Si layers was observed suggesting that at such Al content O does not seem to hinder the n type doping in the material In paper 2 we found the coexistence of two Si DX centers the stable DX1 and the metastable DX2 in Al_xGa_{1-x}N for $x = 0.84$ For the stable DX1 center abrupt deepening of the energy level of the negative charge state DX EDX which determines the ionization energy E_a of the Si donor with increasing of the Al content for $x = 0.83$ was observed The dependence of E_a on the Al content in Al_xGa_{1-x}N Si layers $0.79 < x < 1$ was determined The results explain the drastic decrease of the conductivity as often reported for Al_xGa_{1-x}N Si in previous transport studies For the metastable DX2 center we found that the EDX level remains close to E_d for $x = 0.84$ 1 SiC is a wide band gap semiconductor having high thermal conductivity high breakdown field and large saturated electron drift velocity which are essential properties for high voltage and high power devices In paper 3 the identification of niobium Nb in 4H and 6H SiC grown by high temperature chemical vapor deposition CVD by EPR and theoretical calculations is presented We showed that the incorporated Nb formed

asymmetric split vacancy defect NbSiVC in which Nb locates in a divacancy closer to the Si vacancy and prefers only the hexagonal configuration. In papers 4 and 5 we present the identification and the electronic structure of the negative U Z1 Z2 center in 4H SiC. The Z1 Z2 defect is known to be the most common deep level revealed by Deep Level Transient Spectroscopy (DLTS) in 4H SiC epitaxial layers grown by CVD. The center is also known to be the lifetime killer in as grown CVD material and therefore attracts much attention. Using high doped n type free standing 4H SiC layers irradiated with low energy 250 keV electrons which mainly displace carbon atoms creating C vacancies (VC), C interstitials and their associated defects, it was possible to increase the irradiation dose and hence the defect concentration, allowing the application of EPR and DLTS on the same samples. In paper 4, using EPR, photo EPR, DLTS and capacitance voltage measurements, we showed that the Z1 Z2 center is related to the 2 0 level of VC and its higher lying levels Z1 and Z2 are related to the 0 levels of VC at the hexagonal h and quasi cubic k sites respectively. In paper 5, combining EPR and supercell calculations, the negatively charged VC at the k site was identified. We obtained the excellent agreement in the energy levels of Z1 Z2 determined by DLTS and energy levels of VC calculated by supercell calculations and observed clear negative U behaviors of the negatively charged VC at both k and h sites by EPR measurements, consolidating our assignment of the Z1 Z2 levels to the negatively charged states of VC. In paper 6, we studied a defect related to displaced C atoms in n type 4H SiC irradiated by low energy electrons. In irradiated layers, we observed an EPR center at room temperature. After annealing at temperatures in the range of 300-500 °C, this center transforms to a second configuration which is observed in darkness and can be changed back to the first configuration under illumination. Based on the observed ²⁹Si and ¹³C hyperfine structures, two observed configurations of the EPR center were suggested to be related to different configurations of a carbon interstitial cluster. The annealing bistable behaviors and energy levels of this EPR center are discussed.

Electromagnetic Compatibility Engineering Henry W. Ott, 2011-09-20 Praise for Noise Reduction Techniques in Electronic Systems Henry Ott has literally written the book on the subject of EMC. He not only knows the subject but has the rare ability to communicate that knowledge to others. EE Times Electromagnetic Compatibility Engineering is a completely revised, expanded and updated version of Henry Ott's popular book Noise Reduction Techniques in Electronic Systems. It reflects the most recent developments in the field of electromagnetic compatibility (EMC) and noise reduction and their practical applications to the design of analog and digital circuits in computer, home entertainment, medical, telecom, industrial process control and automotive equipment as well as military and aerospace systems. While maintaining and updating the core information such as cabling, grounding, filtering, shielding, digital circuit grounding and layout, and ESD that made the previous book such a wide success, this new book includes additional coverage of Equipment systems grounding, Switching power supplies and variable speed motor drives, Digital circuit power distribution and decoupling, PCB layout and stack up, Mixed signal PCB layout, RF and transient immunity, Power line disturbances, Precompliance EMC measurements. New

appendices on dipole antennae the theory of partial inductance and the ten most common EMC problems The concepts presented are applicable to analog and digital circuits operating from below audio frequencies to those in the GHz range Throughout the book an emphasis is placed on cost effective EMC designs with the amount and complexity of mathematics kept to the strictest minimum Complemented with over 250 problems with answers Electromagnetic Compatibility Engineering equips readers with the knowledge needed to design electronic equipment that is compatible with the electromagnetic environment and compliant with national and international EMC regulations It is an essential resource for practicing engineers who face EMC and regulatory compliance issues and an ideal textbook for EE courses at the advanced undergraduate and graduate levels

Digital Systems Vahid Asadpour, 2018-11-28 This book provides an approach toward the applications and principle theory of digital signal processing in modern intelligent systems biological engineering telecommunication and information technology Assuming the reader already has prior knowledge of signal processing theory this book will be useful for finding novel methods that fit special needs in digital signal processing DSP The combination of signal processing and intelligent systems in hybrid structures rather than serial or parallel processing provide the best mechanism that is a better fit with the comprehensive nature of human This book is a practical reference that places the emphasis on principles and applications of DSP in digital systems It covers a broad area of digital systems and applications of machine learning methods including convolutional neural networks evolutionary algorithms adaptive filters spectral estimation data compression and functional verification The level of the book is ideal for professional DSP users and useful for graduate students who are looking for solutions to their design problems The theoretical principles provide the required base for comprehension of the methods and application of modifications for the special needs of practical projects

Op Amp Applications Handbook Walt Jung, 2005 A complete and up to date op amp reference for electronics engineers from the most famous op amp guru

Testing for EMC Compliance Mark I. Montrose, Edward M. Nakauchi, 2004-04-08 The Keep It Simple KISS philosophy is the primary focus of this book It is written in very simple language with minimal math as a compilation of helpful EMI troubleshooting hints Its light hearted tone is at odds with the extreme seriousness of most engineering reference works that become boring after a few pages This text tells engineers what to do and how to do it Only a basic knowledge of math electronics and a basic understanding of EMI EMC are necessary to understand the concepts and circuits described Once EMC troubleshooting is demystified readers learn there are quick and simple techniques to solve complicated problems a key aspect of this book Simple and inexpensive methods to resolve EMI issues are discussed to help generate unique ideas and methods for developing additional diagnostic tools and measurement procedures An appendix on how to build probes is included It can be a fun activity even humorous at times with bizarre techniques i e the sticky finger probe

Proceedings of Technical Papers ,1999 *IEEE Transactions on Circuits and Systems* ,2006 *Proceedings* ,2001

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