

European Low-Power Initiative for Electronic System Design

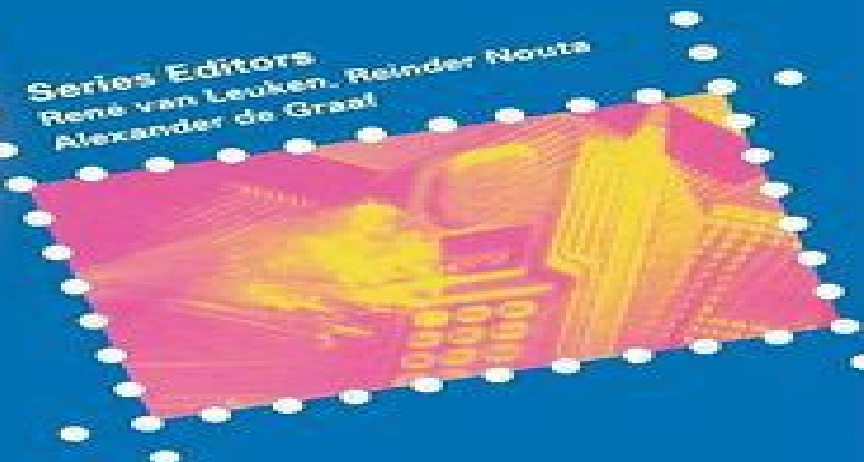
Designing CMOS Circuits for Low Power

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DIMES
Centre for Design of Integrated Micro-Electronic Systems
and Subsystem Technology



Designing Cmos Circuits For Low Power By Dimitrios Soudris

**Dimitrios Soudris, Peter Pirsch, Erich
Barke**



Designing Cmos Circuits For Low Power By Dimitrios Soudris:

Designing CMOS Circuits for Low Power Dimitrios Soudris, Christian Piguet, Costas Goutis, 2002-10-31 Designing CMOS Circuits for Low Power provides the fundamentals of low power design for logic circuit and physical design level as well as the design story of two innovative low power systems developed in the context of European Low Power Initiative for Electronic System Design The main objective is to present in depth analytical and design capabilities for low power design CMOS circuits Determining the sources of power dissipation in depth description of the main existing low power optimization and estimation techniques and their corresponding advantages drawbacks and comparisons are discussed Part I starts with the description of the main principles of dynamic short circuit static and leakage power dissipation together with the low power strategies for reducing each power component A typical low power design flow consists of power optimization and estimation techniques which should be applied in each design level Starting with the formulation of logic optimization problem technology independent and technology dependent power optimization steps for combinational and sequential logic circuits are presented The power characteristics of different logic styles such as dynamic logic and pass transistor logic and alternative implementations of basic digital circuits are studied and compared in terms of performance area and power dissipation Efficient implementations and comparisons of adder and multiplier circuits for various topologies are addressed Furthermore novel techniques that reduce the power based on alternative arithmetic schemes are investigated Then we tackle with the power reduction techniques for SRAM and DRAM memories In the physical design level the power optimization issues of clock distribution interconnect and layout design are described The first part ends up with the advantages and drawbacks of the simulation based and probabilistic power estimation methods of a logic circuit The second part gives the architecture and the design techniques used for the low power implementation of a Safety Critical Application Specific Instruction Processor and ultrasound beamformer application specific integrated circuit Designing CMOS Circuits for Low Power can be used as a textbook for undergraduate and graduate students and VLSI design engineers and professionals from academia and industry who have had a basic knowledge of Microelectronics and CMOS digital design

Low-Power CMOS Circuits Christian Piguet, 2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools addresses the design of low power circuitry in deep submicron technologies It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage

reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers Providing detailed examinations contributed by leading experts Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems

Integrated Circuit Design: Power and Timing Modeling, Optimization and Simulation Dimitrios Soudris, Peter Pirsch, Erich Barke, 2003-06-29 This book constitutes the refereed proceedings of the 10th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2000 held in Gttingen Germany in September 2000 The 33 revised full papers presented were carefully reviewed and selected for inclusion in the book The papers are organized in sections on RTL power modeling power estimation and optimization system level design transistor level design asynchronous circuit design power efficient technologies design of multimedia processing applications adiabatic design and arithmetic modules and analog digital circuit modeling

Low-Power Electronics Design Christian Piguat, 2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today's methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now

VLSI-SoC: Design Methodologies for SoC and SiP Christian Piguat, Ricardo Reis, Dimitrios Soudris, 2010-04-06 This book contains extended and revised versions of the best papers that were presented during the 16th edition of the IFIP IEEE WG10 5 International Conference on Very Large Scale Integration a global System on a Chip Design CAD conference The 16th conference was held at the Grand Hotel of Rhodes Island Greece October 13 15 2008 Previous conferences have taken place in Edinburgh Trondheim Vancouver Munich Grenoble Tokyo Gramado Lisbon Montpellier Darmstadt Perth Nice and Atlanta VLSI SoC 2008 was the 16th in a series of international conferences sponsored by IFIP TC 10 Working Group 10 5 and IEEE CEDA that explores the state of the art and the new developments in the field of VLSI systems and their designs The purpose

of the conference was to provide a forum to exchange ideas and to present industrial and research results in the fields of VLSI ULSI systems embedded systems and croelectronic design and test

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Vassilis Paliouras,Johan Vounckx,Diederik

Verkest,2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops

PATMOS2005wasorganizedbyIMECwithtechnicalco sponsorshipfrom the IEEE Circuits and Systems Society Over the years PATMOS has evolved into an important European event where searchers from both industry and academia discuss and investigate the emerging ch lenges in future and contemporary applications design methodologies and tools quired for the developmentof upcominggenerationsof integrated circuits and systems The technical program of PATMOS 2005 contained state of the art technical contri tions three invited talks a special session on hearing aid design and an embedded torial The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design char terization analysis and optimization in the nanometer era The Technical Program Committee with the assistance of additional expert revi ers selected the 74 papers to be presented at PATMOS The papers were divided into 11 technical sessions and 3 poster sessions As is always the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were carried out per paper Beyond the presentations of the papers the PATMOS technical program was riched by a series of speeches offered by world class experts on important emerging research issues of industrial relevance Prof Jan Rabaey Berkeley USA gave a talk on Traveling the Wild Frontier of Ulta Low Power Design Dr Sung Bae Park S sung gave a presentation on DVL Deep Low Voltage Circuits and Devices Prof

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation José Monteiro,Rene van Leuken,2010-02-18 This book constitutes the thoroughly refereed post conference proceedings of 19th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2009 featuring Integrated Circuit and System Design held in Delft The Netherlands during September 9 11 2009 The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on variability statistical timing circuit level techniques power management low power circuits technology system level techniques power timing optimization techniques self timed circuits low power circuit analysis optimization and low power design studies

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation José L. Ayala,Delong Shang,Alex Yakovlev,2013-01-03 This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design PATMOS 2012 held in Newcastle UK Spain in September 2012 The 25 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems including reconfigurable hardware such as FPGAs The technical program focus on timing performance and

power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization **American Book Publishing Record** ,2003 *Integrated Circuit and System Design. Power and*

Timing Modeling, Optimization and Simulation Johan Vounckx,Nadine Azemard,Philippe Maurine,2006-09-07 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more

IoT for Smart Grids Kostas Siozios,Dimitrios Anagnostos,Dimitrios Soudris,Elias Kosmatopoulos,2018-11-24 This book explains the fundamentals of control theory for Internet of Things IoT systems and smart grids and its applications It discusses the challenges imposed by large scale systems and describes the current and future trends and challenges in decision making for IoT in detail showing the ongoing industrial and academic research in the field of smart grid domain applications It presents step by step design guidelines for the modeling design customisation and calibration of IoT systems applied to smart grids in which the challenges increase with each system s increasing complexity It also provides solutions and detailed examples to demonstrate how to use the techniques to overcome these challenges as well as other problems related to decision making for successful implementation Further it analyses the features of decision making such as low complexity and fault tolerance and uses open source and publicly available software tools to show readers how they can design implement and customise their own system control instantiations This book is a valuable resource for power engineers and researchers as it addresses the analysis and design of flexible decision making mechanisms for smart grids It is also of interest to students on courses related to control of large scale systems since it covers the use of state of the art technology with examples and solutions in every chapter And last but not least it offers practical advice for professionals working with smart grids *Designing 2D and 3D Network-on-Chip Architectures* Konstantinos Tatas,Kostas Siozios,Dimitrios

Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Integrated Circuit and System Design ,2005 **Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation** Rene van Leuken,Gilles Sicard,2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation

high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic

Hardware Accelerators in Data Centers Christoforos Kachris,Babak Falsafi,Dimitrios Soudris,2018-08-21 This book provides readers with an overview of the architectures programming frameworks and hardware accelerators for typical cloud computing applications in data centers The authors present the most recent and promising solutions using hardware accelerators to provide high throughput reduced latency and higher energy efficiency compared to current servers based on commodity processors Readers will benefit from state of the art information regarding application requirements in contemporary data centers computational complexity of typical tasks in cloud computing and a programming framework for the efficient utilization of the hardware accelerators

Scalable Multi-core Architectures Dimitrios Soudris,Axel Jantsch,2011-10-17 As Moore s law continues to unfold two important trends have recently emerged First the growth of chip capacity is translated into a corresponding increase of number of cores Second the parallelization of the computation and 3D integration technologies lead to distributed memory architectures This book describes recent research that addresses urgent challenges in many core architectures and application mapping It addresses the architectural design of many core chips memory and data management power management design and programming methodologies It also describes how new techniques have been applied in various industrial case studies

Fine- and Coarse-Grain Reconfigurable Computing Stamatis Vassiliadis,Dimitrios Soudris,2007-10-12 Fine and Coarse Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine or FPGA and Coarse Grain Reconfigurable Architectures Recently developed integrated architecture design and software supported design flow of FPGA and coarse grain reconfigurable architecture are also described Part I consists of two extensive surveys of FPGA and Coarse Grain Reconfigurable Architectures In Part II case studies innovative research results about reconfigurable architectures and design frameworks from three projects AMDREL MOLEN and ADRES and DRES and a new classification according to microcoded architectural criteria are described Fine and Coarse Grain Reconfigurable Computing is an essential reference for researchers and professionals and can be used as a textbook by undergraduate graduate students and professors

Workload Dependent Mitigation Approaches for Performance Variability Ji-Yung Lin,Michalis Noltsis,Dimitrios Soudris,Francky Catthoor,2025-06-29 This book provides a holistic view of workload dependent mitigation techniques for performance variability The authors describe the use of design time profiling information to reduce the uncertainties in future execution time calculation at run time thereby offering the best option for minimizing system costs while reducing missed deadlines Readers are introduced to an approach that combines dynamic voltage and frequency scaling DVFS with heterogeneous datapaths HDP enabling users to tackle performance variability of multiple timescales down to the sub millisecond level

IEICE Transactions on Electronics,2004

The British National Bibliography Arthur James Wells,2002

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