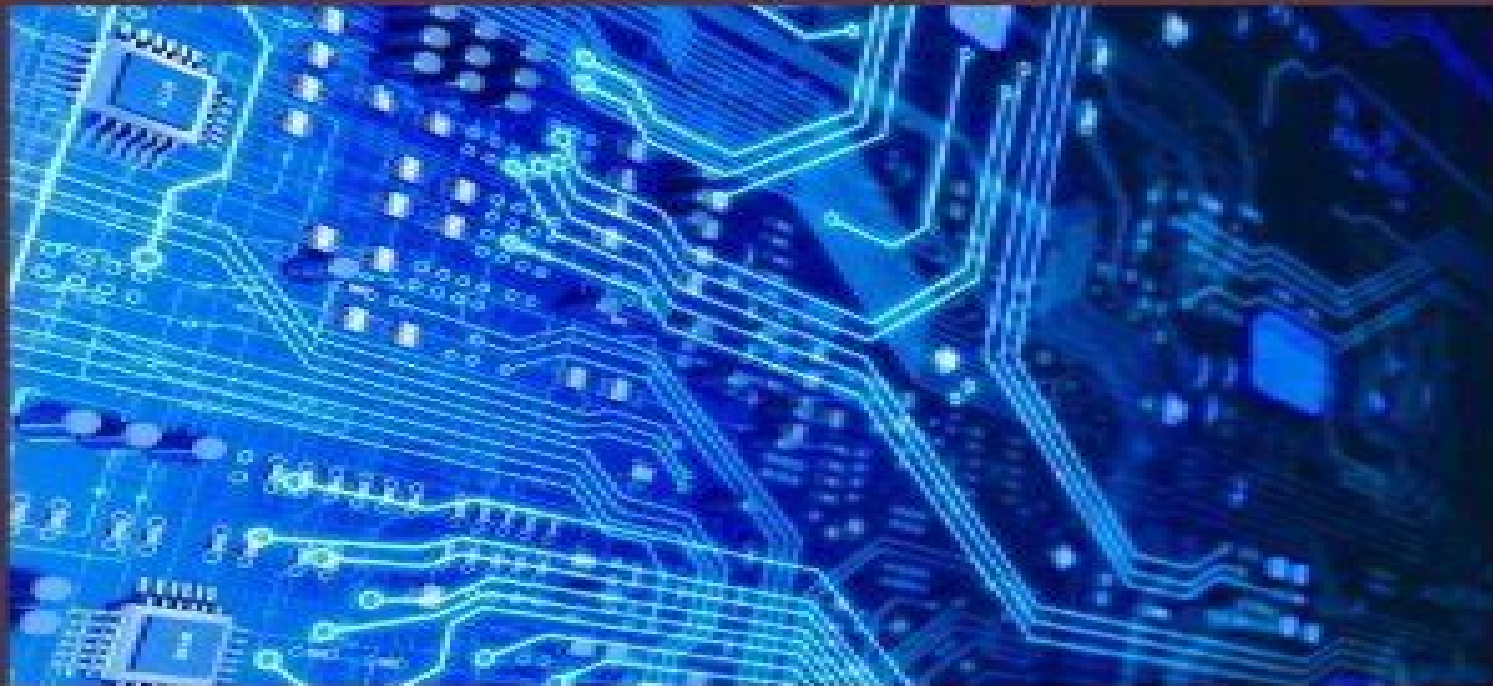


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System-level Test and Validation of Hardware/Software Systems Zebo Peng,2005-04-07 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability Introduction to Advanced System-on-Chip Test Design and Optimization Erik Larsson,2005-11-07 Testing of Integrated Circuits is important to ensure

the production of fault free chips However testing is becoming cumbersome and expensive due to the increasing complexity of these ICs Technology development has made it possible to produce chips where a complete system with an enormous transistor count operating at a high clock frequency is placed on a single die SOC System on Chip The device size miniaturization leads to new fault types the increasing clock frequencies enforces testing for timing faults and the increasing transistor count results in a higher number of possible fault sites Testing must handle all these new challenges in an efficient manner having a global system perspective Test design is applied to make a system testable In a modular core based environment where blocks of reusable logic the so called cores are integrated to a system test design for each core include test method selection test data stimuli and responses generation ATPG definition of test data storage and partitioning off chip as ATE Automatic Test Equipment and or on chip as BIST Built In Self Test wrapper selection and design IEEE std 1500 TAM test access mechanism design and test scheduling minimizing a cost function whilst considering limitations and constraint A system test design perspective that takes all the issues above into account is required in order to develop a globally optimized solution SOC test design and its optimization is the topic of this book It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process

Design of Systems on a Chip: Design and Test
Ricardo Reis, Marcelo Soares Lubaszewski, Jochen A.G. Jess, 2008-11-01 This book is the second of two volumes addressing the design challenges associated with new generations of semiconductor technology The various chapters are compiled from tutorials presented at workshops in recent years by prominent authors from all over the world Technology productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip

Introduction to Advanced System-on-Chip Test Design and Optimization Erik Larsson, 2008-11-01 SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test

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