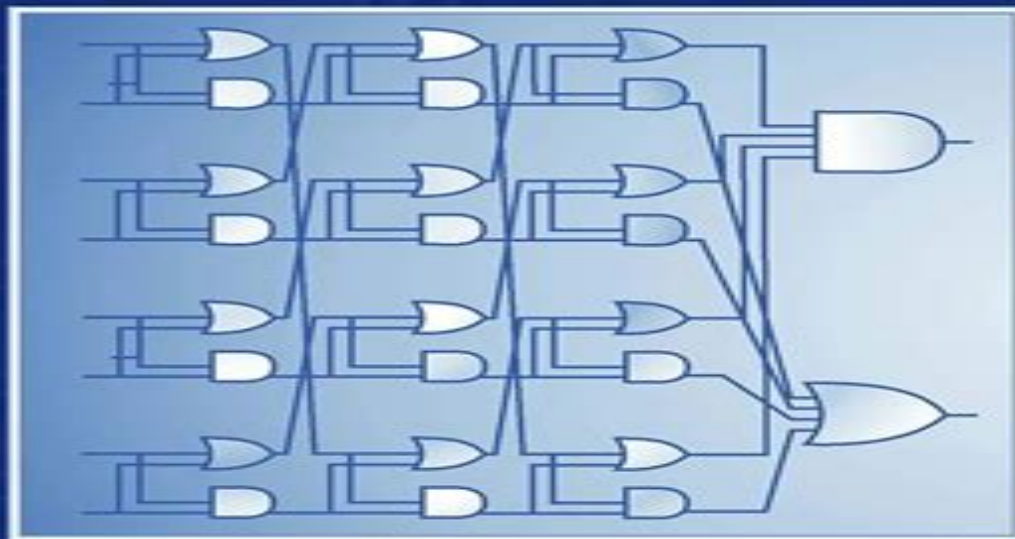


FAULT TOLERANT AND FAULT TESTABLE HARDWARE DESIGN



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Fault Tolerant & Fault Testable Hardware Design Lala,1985 Fault-Tolerant Design Elena Dubrova,2013-03-15 This textbook serves as an introduction to fault tolerance intended for upper division undergraduate students graduate level students and practicing engineers in need of an overview of the field Readers will develop skills in modeling and evaluating fault tolerant architectures in terms of reliability availability and safety They will gain a thorough understanding of fault tolerant computers including both the theory of how to design and evaluate them and the practical knowledge of achieving fault tolerance in electronic communication and software systems Coverage includes fault tolerance techniques through hardware software information and time redundancy The content is designed to be highly accessible including numerous examples and exercises Solutions and powerpoint slides are available for instructors *Design and Analysis of Fault-tolerant Digital Systems* Barry W. Johnson,1989 *Fault Tolerant and Fault Testable Hardware* Parag K. Lala,1985

Hardware and Software Architectures for Fault Tolerance Michel Banatre,1994-02-28 Fault tolerance has been an active research area for many years This volume presents papers from a workshop held in 1993 where a small number of key researchers and practitioners in the area met to discuss the experiences of industrial practitioners to provide a perspective on the state of the art of fault tolerance research to determine whether the subject is becoming mature and to learn from the experiences so far in order to identify what might be important research topics for the coming years The workshop provided a more intimate environment for discussions and presentations than usual at conferences The papers in the volume were presented at the workshop then updated and revised to reflect what was learned at the workshop Self-Checking and Fault-Tolerant Digital Design Parag K. Lala,2001 With VLSI chip transistors getting smaller and smaller today s digital systems are more complex than ever before This increased complexity leads to more cross talk noise and other sources of transient errors during normal operation Traditional off line testing strategies cannot guarantee detection of these transient faults And with critical applications relying on faster more powerful chips fault tolerant self checking mechanisms must be built in to assure reliable operation Self Checking and Fault Tolerant Digital Design deals extensively with self checking design techniques and is the only book that emphasizes major techniques for hardware fault tolerance Graduate students in VLSI design courses as well as practicing designers will appreciate this balanced treatment of the concepts and theory underlying fault tolerance along with the practical techniques used to create fault tolerant systems Features Introduces reliability theory and the importance of maintainability Presents coding and the construction of several error detecting and correcting codes Discusses in depth the available techniques for fail safe design of combinational circuits Details checker design techniques for detecting erroneous bits and encoding output of self checking circuits Demonstrates how to design self checking sequential circuits including a technique for fail safe state machine design **Fault Tolerance, Principles and**

Practice P. A. Lee, Thomas Anderson, Tom Anderson, 1990 **Software-Implemented Hardware Fault Tolerance** Olga Goloubeva, Maurizio Rebaudengo, Matteo Sonza Reorda, Massimo Violante, 2006-09-19 Software Implemented Hardware Fault Tolerance addresses the innovative topic of software implemented hardware fault tolerance SIHFT i.e. how to deal with faults affecting the hardware by only or mainly acting on the software The first SIHFT techniques were proposed and adopted several decades ago but they have been the object of new interest in the past few years mainly due to the need for developing low cost safety critical computer based applications in fields such as automotive biomedics and telecommunications Therefore several new approaches to detect and when possible correct transient and permanent faults in the hardware have been recently proposed These approaches are innovative with respect to those proposed in the past since they are of higher applicability often starting from the source level code of an application and generality being capable of coping with many different fault types The book presents the theory behind software implemented hardware fault tolerance as well as the practical aspects related to put it at work on real examples By evaluating accurately the advantages and disadvantages of the already available approaches the book provides a guide to developers willing to adopt software implemented hardware fault tolerance in their applications Moreover the book identifies open issues for researchers willing to improve the already available techniques *Fault Tolerant and Fault Testable Hardware Design* Parag K. Lala, 1985 **Fault-tolerant Systems** Israel Koren, C. Mani Krishna, 2007 There are many applications in which the reliability of the overall system must be far higher than the reliability of its individual components In such cases designers devise mechanisms and architectures that allow the system to either completely mask the effects of a component failure or recover from it so quickly that the application is not seriously affected This is the work of fault tolerant designers and their work is increasingly important and complex not only because of the increasing number of mission critical applications but also because the diminishing reliability of hardware means that even systems for non critical applications will need to be designed with fault tolerance in mind Reflecting the real world challenges faced by designers of these systems this book addresses fault tolerance design with a systems approach to both hardware and software No other text on the market takes this approach nor offers the comprehensive and up to date treatment Koren and Krishna provide Students designers and architects of high performance processors will value this comprehensive overview of the field The first book on fault tolerance design with a systems approach Comprehensive coverage of both hardware and software fault tolerance as well as information and time redundancy Incorporated case studies highlight six different computer systems with fault tolerance techniques implemented in their design Available to lecturers is a complete ancillary package including online solutions manual for instructors and PowerPoint slides Software-implemented Hardware Fault Tolerance, 2010 Hardware and Software Architectures for Fault Tolerance Michel Banatre, Peter A. Lee, 2014-09-11 Fault Tolerant System Design S?c Levi, Shem-Tov Levi, Ashok K. Agrawala, 1994 **Fault-tolerant Hardware Designs and Their Reliability Analysis** Mahmoud Hafezparast, 1990

Modeling Hardware and Software Fault Tolerant Systems Lorrie A. Tomek,1996 *Design and Analysis of Fault Tolerant Digital Systems* B. W. Johnson,1991-01-01 *Implementation of a Fault Tolerant Computing Testbed* David C. Summers,2000-06-01

With spacecraft designs placing more emphasis on reduced cost faster design time and higher performance it is easy to understand why more commercial off the shelf COTS devices are being used in space based applications The COTS devices offer spacecraft designers shorter design to orbit times lower system costs orders of magnitude better performance and a much better software availability than their radiation hardened radhard counterparts The major drawback to using COTS devices in space is their increased susceptibility to the effects of radiation single event upsets SEUs in particular This thesis will focus on the implementation of a fault tolerant computer system The hardware design presented here has two different benefits First the system can act as a software testbed which allows testing of software fault tolerant techniques in the presence of radiation induced SEUs This allows the testing of the software algorithms in the environment they were designed to operate in without the expense of being placed in orbit Additionally the design can be used as a hybrid fault tolerant computer system By combining the masking ability of the hardware with supporting software the system can mask out and reset processor errors in real time The design layout will be presented using OrCAD schematics A second generation experiment in fault-tolerant software John C. Knight,1986

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