

CHAPTER 1 INTRODUCTION

1.1

An ADDSUBTRACT logic circuit is shown below. It performs the ADD operation for $P = 0$, and SUBTRACT for $P = 1$.

- (a) Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for transmission gates and XNORs, are inverting. For example, AND gate is implemented with NAND followed by an inverter.
- (b) By using the gate array platform given on page 47, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.

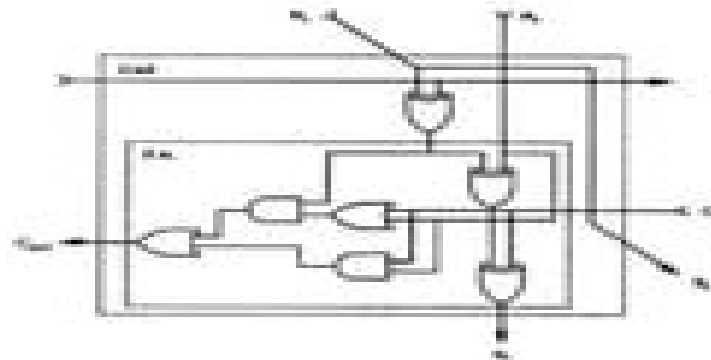


Figure P14.5(a)

SOLUTION:

- (b) The CMOS circuit implementation using the gate array platform:

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Table of Contents Cmos Digital Integrated Circuits Manual

1. Understanding the eBook Cmos Digital Integrated Circuits Manual
 - The Rise of Digital Reading Cmos Digital Integrated Circuits Manual
 - Advantages of eBooks Over Traditional Books
2. Identifying Cmos Digital Integrated Circuits Manual
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Cmos Digital Integrated Circuits Manual
 - User-Friendly Interface
4. Exploring eBook Recommendations from Cmos Digital Integrated Circuits Manual
 - Personalized Recommendations

- Cmos Digital Integrated Circuits Manual User Reviews and Ratings
- Cmos Digital Integrated Circuits Manual and Bestseller Lists
- 5. Accessing Cmos Digital Integrated Circuits Manual Free and Paid eBooks
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 - Cmos Digital Integrated Circuits Manual Budget-Friendly Options
- 6. Navigating Cmos Digital Integrated Circuits Manual eBook Formats
 - ePub, PDF, MOBI, and More
 - Cmos Digital Integrated Circuits Manual Compatibility with Devices
 - Cmos Digital Integrated Circuits Manual Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Cmos Digital Integrated Circuits Manual
 - Highlighting and Note-Taking Cmos Digital Integrated Circuits Manual
 - Interactive Elements Cmos Digital Integrated Circuits Manual
- 8. Staying Engaged with Cmos Digital Integrated Circuits Manual
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Cmos Digital Integrated Circuits Manual
- 9. Balancing eBooks and Physical Books Cmos Digital Integrated Circuits Manual
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Cmos Digital Integrated Circuits Manual
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Cmos Digital Integrated Circuits Manual
 - Setting Reading Goals Cmos Digital Integrated Circuits Manual
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Cmos Digital Integrated Circuits Manual
 - Fact-Checking eBook Content of Cmos Digital Integrated Circuits Manual

- Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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