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Chip Design for Submicron VLSI:

CMOS Layout and Simulation

John P. Uyemura



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Chip Design For Submicron Vlsi Cmos Layout And

Rob A. Rutenbar, Georges G. E. Gielen



Chip Design For Submicron Vlsi Cmos Layout And:

Chip Design for Submicron VLSI John Paul Uyemura, 2006 This book teaches the principles of physical design layout and simulation of CMOS integrated circuits It is written around a very powerful CAD program called Microwind that is available on the accompanying CD ROM Featuring a friendly interface Microwind is both educational and useful for designing CMOS chips

Chip Design For Submicron Vlsi: Cmos Layout & Simulation Umura, **MOSFET Technologies for Double-Pole Four-Throw Radio-Frequency Switch** Viranjay M. Srivastava, Ghanshyam Singh, 2013-10-07 This book provides analysis and discusses the design of various MOSFET technologies which are used for the design of Double Pole Four Throw DP4T RF switches for next generation communication systems The authors discuss the design of the DP4T RF switch by using the Double Gate DG MOSFET as well as the Cylindrical Surrounding double gate CSDG MOSFET The effect of HfO₂ high dielectric material in the design of DG MOSFET and CSDG MOSFET is also explored Coverage includes comparison of Single gate MOSFET and Double gate MOSFET switching parameters as well as testing of MOSFETs parameters using image acquisition

Handbook of VLSI Chip Design and Expert Systems A. F. Schwarz, 2014-05-10 Handbook of VLSI Chip Design and Expert Systems provides information pertinent to the fundamental aspects of expert systems which provides a knowledge based approach to problem solving This book discusses the use of expert systems in every possible subtask of VLSI chip design as well as in the interrelations between the subtasks Organized into nine chapters this book begins with an overview of design automation which can be identified as Computer Aided Design of Circuits and Systems CAD/CAS This text then presents the progress in artificial intelligence with emphasis on expert systems Other chapters consider the impact of design automation which exploits the basic capabilities of computers to perform complex calculations and to handle huge amounts of data with a high speed and accuracy This book discusses as well the characterization of microprocessors The final chapter deals with interactive I/O devices This book is a valuable resource for system design experts circuit analysts and designers logic designers device engineers technologists and application specific designers

Introduction to Place and Route Design in VLSIs Patrick Lee, 2007-01-05 The book is organized in seven chapters Physical design flow Timing constraints Place and route concepts Tool vendors Process constraints Timing closure Place and route methodology and flow ECO and spare gates Formal verification Coupling noise Chip optimization and tapeout

Introduction to Physical Integration and Tapeout in VLSIs Patrick Lee, 2010-04-27 This book covers issues and solutions in the physical integration and tapeout management for VLSI design Chapter 1 gives the overview Chapter 2 shows detailed techniques for physical design Chapter 3 provides CAD flows Chapter 4 discusses on chip interconnects A glossary of keywords is provided at the end

Introduction to VLSI Systems Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder

problems requires fundamental understanding of circuit and layout design issues Furthermore engineers can often develop their physical intuition to estimate the behavior of circuits rapidly without relying predominantly on computer aided design CAD tools Introduction to VLSI Systems A Logic Circuit and System Perspective addresses the need for teaching such a topic in terms of a logic circuit and system design perspective To achieve the above mentioned goals this classroom tested book focuses on Implementing a digital system as a full custom integrated circuit Switch logic design and useful paradigms that may apply to various static and dynamic logic families The fabrication and layout designs of complementary metal oxide semiconductor CMOS VLSI Important issues of modern CMOS processes including deep submicron devices circuit optimization interconnect modeling and optimization signal integrity power integrity clocking and timing power dissipation and electrostatic discharge ESD Introduction to VLSI Systems builds an understanding of integrated circuits from the bottom up paying much attention to logic circuit layout and system designs Armed with these tools readers can not only comprehensively understand the features and limitations of modern VLSI technologies but also have enough background to adapt to this ever changing field

Power Distribution Network Design for VLSI Qing K. Zhu, 2004-02-19 A hands on troubleshooting guide for VLSI network designers The primary goal in VLSI very large scale integration power network design is to provide enough power lines across a chip to reduce voltage drops from the power pads to the center of the chip Voltage drops caused by the power network s metal lines coupled with transistor switching currents on the chip cause power supply noises that can affect circuit timing and performance thus providing a constant challenge for designers of high performance chips Power Distribution Network Design for VLSI provides detailed information on this critical component of circuit design and physical integration for high speed chips A vital tool for professional engineers especially those involved in the use of commercial tools as well as graduate students of engineering the text explains the design issues guidelines and CAD tools for the power distribution of the VLSI chip and package and provides numerous examples for its effective application Features of the text include An introduction to power distribution network design Design perspectives such as power network planning layout specifications decoupling capacitance insertion modeling and analysis Electromigration phenomena IR drop analysis methodology Commands and user interfaces of the VoltageStorm TM CAD tool Microprocessor design examples using on chip power distribution Flip chip and package design issues Power network measurement techniques from real silicon The author includes several case studies and a glossary of key words and basic terms to help readers understand and integrate basic concepts in VLSI design and power distribution

Signal Integrity Effects in Custom IC and ASIC Designs Raminderpal Singh, 2001-12-12 offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity Jake Buurma Senior Vice President Worldwide Research Development Cadence Design Systems Inc Covers signal integrity effects in high performance Radio Frequency RF IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD

managers now and in the future A Wiley IEEE Press publication *Nano-CMOS Circuit and Physical Design* Ban Wong, Anurag Mittal, Yu Cao, Greg W. Starr, 2005-04-08 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation **Transient-Induced Latchup in CMOS Integrated Circuits** Ming-Dou Ker, Sheng-Fu Hsu, 2009-07-23 The book all semiconductor device engineers must read to gain a practical feel for latchup induced failure to produce lower cost and higher density chips Transient Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup explaining the critical issues that have resurfaced for CMOS technologies Once readers can gain an understanding of the standard practices for TLU Ker and Hsu discuss the physical mechanism of TLU under a system level ESD test while introducing an efficient component level TLU measurement setup The authors then present experimental methodologies to extract safe and area efficient compact layout rules for latchup prevention including layout rules for I O cells internal circuits and between I O and internal circuits The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18 micrometer 1.8V/3.3V silicided CMOS process Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time to market Written by experts with real world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system level ESD and EFT tests This book is essential for practicing engineers involved in IC design IC design management system and application design reliability and failure analysis Undergraduate and postgraduate students specializing in CMOS circuit design and layout will find this book to be a valuable introduction to real world industry problems and a key reference during the course of their careers **Computer-Aided Design of Analog Integrated Circuits and Systems** Rob A. Rutenbar, Georges G. E. Gielen, 2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years

ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today's new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck *EDA for IC Implementation, Circuit Design, and Process Technology* Luciano Lavagno, Louis Scheffer, Grant Martin, 2018-10-03

Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The second volume EDA for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic to GDSII a file format used to transfer data of semiconductor physical layout analog mixed signal design physical verification and technology CAD TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale power supply network design and analysis design modeling and much more Save on the complete set **Power Distribution**

Networks with On-Chip Decoupling Capacitors Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba, Selçuk Köse, Eby G. Friedman, 2010-11-23 This book describes methods for distributing power in high speed high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt It provides a broad and cohesive treatment of power distribution systems and related design problems including both circuit network models and design techniques for on chip decoupling capacitors providing insight and intuition into the behavior and design of on chip power distribution systems Organized into subareas to provide a more intuitive flow to the reader this second edition adds more than a hundred pages of new content including inductance models for interdigitated structures design strategies for multi layer power grids advanced methods for efficient power grid design and analysis and methodologies for simultaneously placing on chip multiple power supplies and decoupling capacitors The emphasis of this additional material is on managing the complexity of on chip power distribution networks **On-Chip Communication Architectures** Sudeep Pasricha, Nikil Dutt, 2010-07-28

Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research

and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that will have a significant impact on research and design of communication architectures over the next several years Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology

Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals *On-Chip Power Delivery and Management* Inna P. Vaisband,Renatas Jakushokas,Mikhail Popovich,Andrey V. Mezhiba,Selçuk Köse,Eby G.

Friedman,2016-04-26 This book describes methods for distributing power in high speed high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt It provides a broad and cohesive treatment of power delivery and management systems and related design problems including both circuit network models and design techniques for on chip decoupling capacitors providing insight and intuition into the behavior and design of on chip power distribution systems Organized into subareas to provide a more intuitive flow to the reader this fourth edition adds more than a hundred pages of new content including inductance models for interdigitated structures design strategies for multi layer power grids advanced methods for efficient power grid design and analysis and methodologies for simultaneously placing on chip multiple power supplies and decoupling capacitors The emphasis of this additional material is on managing the complexity of on chip power distribution networks *VLSI-SOC: From Systems to Chips* Manfred Glesner,2006-05-17 This

book contains extended and revised versions of the best papers that have been presented during the twelfth edition of the IFIP TC10 WG10 5 International Conference on Very Large Scale Integration a Global System on a Chip Design CAD Conference The 12 edition was held at the Lufthansa Training Center in Seeheim Jugenheim south of Darmstadt Germany December 1 3 2003 Previous conferences have taken place in Edinburgh 81 Trondheim 83 Tokyo 85 Vancouver 87 Munich 89 Edinburgh 91 Grenoble 93 Tokyo 95 Gramado 97 Lisbon 99 and Montpellier 01 The purpose of this conference sponsored by IFIP TC 10 Working Group 10 5 is to provide a forum to exchange ideas and show research results in the field of microelectronics design The current trend toward increasing chip integration brings about exhilarating new challenges both at the physical and system design levels this conference aims to address these exciting new issues The 2003 edition of VLSI SoC conserved the traditional structure which has been successful in previous editions The quality of submissions 142 papers made the selection process difficult but finally 57 papers and 14 posters were accepted for presentation in VLSI SoC 2003 Submissions came from Austria Bulgaria Brazil Canada Egypt England Estonia Finland France Germany Greece Hungary India Iran Israel Italy Japan Korea Malaysia Mexico Netherlands Poland Portugal Romania Spain Sweden Taiwan and the United States of America From 57 papers presented at the conference 18 were selected to have an extended and revised version included in this book

A Practical Approach to VLSI System on Chip (SoC) Design Veena S.

Chakravarthi, 2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale

A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs

Low Power Design in Deep Submicron Electronics W. Nebel, Jean Mermet, 2013-06-29 Low Power Design in Deep Submicron Electronics deals with the different aspects of low power design for deep submicron electronics at all levels of abstraction from system level to circuit level and technology Its objective is to guide industrial and academic engineers and researchers in the selection of methods technologies and tools and to provide a baseline for further developments Furthermore the book has been written to serve as a textbook for postgraduate student courses In order to achieve both goals it is structured into different chapters each of which addresses a different phase of the design a particular level of abstraction a unique design style or technology These design related chapters are amended by

motivations in Chapter 2 which presents visions both of future low power applications and technology advancements and by some advanced case studies in Chapter 9 From the Foreword This global nature of design for low power was well understood by Wolfgang Nebel and Jean Mermet when organizing the NATO workshop which is the origin of the book They invited the best experts in the field to cover all aspects of low power design As a result the chapters in this book are covering deep submicron CMOS digital system design for low power in a systematic way from process technology all the way up to software design and embedded software systems Low Power Design in Deep Submicron Electronics is an excellent guide for the practicing engineer the researcher and the student interested in this crucial aspect of actual CMOS design It contains about a thousand references to all aspects of the recent five years of feverish activity in this exciting aspect of design Hugo de Man Professor K U Leuven Belgium Senior Research Fellow IMEC Belgium

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