Synthesis Lectures on
Computer Architecture

SYNTHESIS
COLLECTION OF TECHNOLOGY

Hari Angepat · Derek Chiou · Eric S. Chung
James C. Hoe

FPGA-Accelerated Simulation of Computer System

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FPGA-Accelerated Simulation of Computer Systems Hari Angepat,Derek Chiou,Eric S. Chung,James C. Hoe,2014-07-01 To date the most common form of simulators of computer systems are software based running on standard computers One promising approach to improve simulation performance is to apply hardware specifically reconfigurable hardware in the form of field programmable gate arrays FPGAs This manuscript describes various approaches of using FPGAs to accelerate software implemented simulation of computer systems and selected simulators that incorporate those techniques More precisely we describe a simulation architecture taxonomy that incorporates a simulation architecture specifically designed for FPGA accelerated simulation survey the state of the art in FPGA accelerated simulation and describe in detail selected instances of the described techniques Table of Contents Preface Acknowledgments Introduction Simulator Background Accelerating Computer System Simulators with FPGAs Simulation Virtualization Categorizing FPGA based Simulators Conclusion Bibliography Authors Biographies FPGA-Accelerated Simulation of Computer Systems Hari Angepat,Derek Chiou,Eric S. Chung,James C. Hoe,2022-05-31 To date the most common form of simulators of computer systems are software based running on standard computers One promising approach to improve simulation performance is to apply hardware specifically reconfigurable hardware in the form of field programmable gate arrays FPGAs This manuscript describes various approaches of using FPGAs to accelerate software implemented simulation of computer systems and selected simulators that incorporate those techniques More precisely we describe a simulation architecture taxonomy that incorporates a simulation architecture specifically designed for FPGA accelerated simulation survey the state of the art in FPGA accelerated simulation and describe in detail selected instances of the described techniques Table of Contents Preface Acknowledgments Introduction Simulator Background Accelerating Computer System Simulators with FPGAs Simulation Virtualization Categorizing FPGA based Simulators Conclusion Bibliography Authors Biographies **Quantum Computer Systems** Yongshan Ding,Frederic T. Chong,2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing **Customizable Computing** Yu-Ting Chen,Jason Cong,Michael Gill,Glenn Reinman,Bingjun Xiao,2022-05-31 Since the end of Dennard scaling in the early

2000s improving the energy efficiency of computation has been the main concern of the research community and industry The large energy efficiency gap between general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their impact on performance and energy efficiency We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful reference basis for further research design and implementation for large scale deployment in future computing systems **Robotic Computing on FPGAs** Shaoshan Liu,Zishen Wan,Bo Yu,Yu Wang,2022-05-31 This book provides a thorough overview of the state of the art field programmable gate array FPGA based robotic computing accelerator designs and summarizes their adopted optimized techniques This book consists of ten chapters delving into the details of how FPGAs have been utilized in robotic perception localization planning and multi robot collaboration tasks In addition to individual robotic tasks this book provides detailed descriptions of how FPGAs have been used in robotic products including commercial autonomous vehicles and space exploration robots Space-Time Computing with Temporal Neural Networks James E. Smith,2022-05-31 Understanding and implementing the brain s computational paradigm is the one true grand challenge facing computer researchers Not only are the brain s computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain s computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain s neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input

patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described

In-/Near-Memory Computing Daichi Fujiki,Xiaowei Wang,Arun Subramaniyan,Reetuparna Das,2022-05-31 This book provides a structured introduction of the key concepts and techniques that enable in near memory computing For decades processing in memory or near memory computing has been attracting growing interest due to its potential to break the memory wall Near memory computing moves compute logic near the memory and thereby reduces data movement Recent work has also shown that certain memories can morph themselves into compute units by exploiting the physical properties of the memory cells enabling in situ computing in the memory array While in and near memory computing can circumvent overheads related to data movement it comes at the cost of restricted flexibility of data representation and computation design challenges of compute capable memories and difficulty in system and software integration Therefore wide deployment of in near memory computing cannot be accomplished without techniques that enable efficient mapping of data intensive applications to such devices without sacrificing accuracy or increasing hardware costs excessively This book describes various memory substrates amenable to in and near memory computing architectural approaches for designing efficient and reliable computing devices and opportunities for in near memory acceleration of different classes of applications **Deep Learning Systems** Andres Rodriguez,2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler

techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to bettercollaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book **Compiling Algorithms for Heterogeneous Systems** Steven Bell,Jing Pu,James Hegarty,Mark Horowitz,2022-05-31 Most emerging applications in imaging and machine learning must perform immense amounts of computation while holding to strict limits on energy and power To meet these goals architects are building increasingly specialized compute engines tailored for these specific tasks The resulting computer systems are heterogeneous containing multiple processing cores with wildly different execution models Unfortunately the cost of producing this specialized hardware and the software to control it is astronomical Moreover the task of porting algorithms to these heterogeneous machines typically requires that the algorithm be partitioned across the machine and rewritten for each specific architecture which is time consuming and prone to error Over the last several years the authors have approached this problem using domain specific languages DSLs high level programming languages customized for specific domains such as database manipulation machine learning or image processing By giving up generality these languages are able to provide high level abstractions to the developer while producing high performance output The purpose of this book is to spur the adoption and the creation of domain specific languages especially for the task of creating hardware designs In the first chapter a short historical journey explains the forces driving computer architecture today Chapter 2 describes the various methods for producing designs for accelerators outlining the push for more abstraction and the tools that enable designers to work at a higher conceptual level From there Chapter 3 provides a brief introduction to image processing algorithms and hardware design patterns for implementing them Chapters 4 and 5 describe and compare Darkroom and Halide two domain specific languages created for image processing that produce high performance designs for both FPGAs and CPUs from the same source code enabling rapid design cycles and quick porting of algorithms The final section describes how the DSL approach also simplifies the problem of interfacing between application code and the accelerator by generating the driver stack in addition to the accelerator configuration This book should serve as a useful introduction to domain specialized computing for computer architecture students and as a primer on domain specific languages and image processing hardware

for those with more experience in the field *Innovations in the Memory System* Rajeev Balasubramonian,2022-05-31 The memory system has the potential to be a hub for future innovation While conventional memory systems focused primarily on high density other memory system metrics like energy security and reliability are grabbing modern research headlines With processor performance stagnating it is also time to consider new programming models that move some application computations into the memory system This in turn will lead to feature rich memory systems with new interfaces The past decade has seen a number of memory system innovations that point to this future where the memory system will be much more than dense rows of unintelligent bits This book takes a tour through recent and prominent research works touching upon new DRAM chip designs and technologies near data processing approaches new memory channel architectures techniques to tolerate the overheads of refresh and fault tolerance security attacks and mitigations and memory scheduling

Architectural and Operating System Support for Virtual Memory Abhishek Bhattacharjee,Daniel Lustig,2022-05-31 This book provides computer engineers academic researchers new graduate students and seasoned practitioners an end to end overview of virtual memory We begin with a recap of foundational concepts and discuss not only state of the art virtual memory hardware and software support available today but also emerging research trends in this space The span of topics covers processor microarchitecture memory systems operating system design and memory allocation We show how efficient virtual memory implementations hinge on careful hardware and software cooperation and we discuss new research directions aimed at addressing emerging problems in this space Virtual memory is a classic computer science abstraction and one of the pillars of the computing revolution It has long enabled hardware flexibility software portability and overall better security to name just a few of its powerful benefits Nearly all user level programs today take for granted that they will have been freed from the burden of physical memory management by the hardware the operating system device drivers and system libraries However despite its ubiquity in systems ranging from warehouse scale datacenters to embedded Internet of Things IoT devices the overheads of virtual memory are becoming a critical performance bottleneck today Virtual memory architectures designed for individual CPUs or even individual cores are in many cases struggling to scale up and scale out to today s systems which now increasingly include exotic hardware accelerators such as GPUs FPGAs or DSPs and emerging memory technologies such as non volatile memory and which run increasingly intensive workloads such as virtualized and or big data applications As such many of the fundamental abstractions and implementation approaches for virtual memory are being augmented extended or entirely rebuilt in order to ensure that virtual memory remains viable and performant in the years to come An Open-Source Research Platform for Heterogeneous Systems on Chip Andreas Dominic Kurth,2022-10-05 Heterogeneous systems on chip HeSoCs combine general purpose feature rich multi core host processors with domain specific programmable many core accelerators PMCAs to unite versatility with energy efficiency and peak performance By virtue of their heterogeneity HeSoCs hold the promise of increasing performance and energy efficiency

compared to homogeneous multiprocessors because applications can be executed on hardware that is designed for them However this heterogeneity also increases system complexity substantially This thesis presents the first research platform for HeSoCs where all components from accelerator cores to application programming interface are available under permissive open source licenses We begin by identifying the hardware and software components that are required in HeSoCs and by designing a representative hardware and software architecture We then design implement and evaluate four critical HeSoC components that have not been discussed in research at the level required for an open source implementation First we present a modular topology agnostic high performance on chip communication platform which adheres to a state of the art industry standard protocol We show that the platform can be used to build high bandwidth e g 2 5 GHz and 1024 bit data width end to end communication fabrics with high degrees of concurrency e g up to 256 independent concurrent transactions Second we present a modular and efficient solution for implementing atomic memory operations in highly scalable many core processors which demonstrates near optimal linear throughput scaling for various synthetic and real world workloads and requires only 0 5 kGE per core Third we present a hardware software solution for shared virtual memory that avoids the majority of translation lookaside buffer misses with prefetching supports parallel burst transfers without additional buffers and can be scaled with the workload and number of parallel processors Our work improves accelerator performance for memory intensive kernels by up to 4 Fourth we present a software toolchain for mixed data model heterogeneous compilation and OpenMP offloading Our work enables transparent memory sharing between a 64 bit host processor and a 32 bit accelerator at overheads below 0 7 % compared to 32 bit only execution Finally we combine our contributions to a research platform for state of the art HeSoCs and demonstrate its performance and flexibility AI for Computer Architecture Lizhong Chen,Drew Penney,Daniel Jiménez,2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs **The Datacenter as a Computer** Luiz André Barroso,Urs Hölzle,Parthasarathy Ranganathan,2022-06-01 This book describes warehouse scale computers WSCs the computing platforms that power cloud computing and all the great web services we use every day It discusses how these new systems treat the datacenter itself as one massive computer designed at warehouse scale with hardware and software working in

concert to deliver good levels of internet service performance The book details the architecture of WSCs and covers the main factors influencing their design operation and cost structure and the characteristics of their software base Each chapter contains multiple real world examples including detailed case studies and previously unpublished details of the infrastructure used to power Google s online services Targeted at the architects and programmers of today s WSCs this book provides a great foundation for those looking to innovate in this fascinating and important area but the material will also be broadly interesting to those who just want to understandthe infrastructure powering the internet The third edition reflects four years of advancements since the previous edition and nearly doubles the number of pictures and figures New topics range from additional workloads like video streaming machine learning and public cloud to specialized silicon accelerators storage and network building blocks and a revised discussion of data center power and cooling and uptime Further discussions of emerging trends and opportunities ensure that this revised edition will remain an essential resource for educators and professionals working on the next generation of WSCs **Deep Learning for Computer Architects** Brandon Reagen,Robert Adolf,Paul Whatmough,Gu-Yeon Wei,David Brooks,2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context Power-Efficient Computer Architectures Magnus Själander,Margaret Martonosi,Stefanos Kaxiras,2022-05-31 As Moore s Law and Dennard scaling trends have slowed the challenges of building high performance computer architectures while maintaining acceptable power efficiency levels have heightened Over the past ten years architecture techniques for power efficiency have shifted from primarily focusing on module level efficiencies toward more holistic design styles based on parallelism and heterogeneity This work highlights and synthesizes recent

techniques and trends in power efficient computer architecture Table of Contents Introduction Voltage and Frequency Management Heterogeneity and Specialization Communication and Memory Systems Conclusions Bibliography Authors Biographies **On-Chip Networks, Second Edition** Natalie Enright Jerger,Tushar Krishna,Li-Shiuan Peh,2022-05-31 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value to both graduate students and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For example these fundamental concepts include message passing multicast routing and bubble flow control schemes **Data Orchestration in Deep Learning Accelerators** Tushar Krishna,Hyoukjun Kwon,Angshuman Parashar,Michael Pellauer,Ananda Samajdar,2022-05-31 This Synthesis Lecture focuses on techniques for efficient data orchestration within DNN accelerators The End of Moore s Law coupled with the increasing growth in deep learning and other AI applications has led to the emergence of custom Deep Neural Network DNN accelerators for energy efficient inference on edge devices Modern DNNs have millions of hyper parameters and involve billions of computations this necessitates extensive data movement from memory to on chip processing engines It is well known that the cost of data movement today surpasses the cost of the actual computation therefore DNN accelerators require careful orchestration of data across on chip compute network and memory elements to minimize the number of accesses to external DRAM The book covers DNN dataflows data reuse buffer hierarchies networks on chip and automated design space exploration It concludes with data orchestration challenges with compressed and sparse DNNs and future trends The target audience is students engineers and researchers interested in designing high performance and low energy accelerators for DNN inference **On-Chip Networks** Natalie Enright Jerger,Tushar Krishna,Li-Shiuan Peh,2017-06-19 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value to both graduate students

and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For example these fundamental concepts include message passing multicast routing and bubble flow control schemes **Efficient Processing of Deep Neural Networks** Vivienne Sze,Yu-Hsin Chen,Tien-Ju Yang,Joel S. Emer,2022-05-31 This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks DNNs DNNs are currently widely used for many artificial intelligence AI applications including computer vision speech recognition and robotics While DNNs deliver state of the art accuracy on many AI tasks it comes at the cost of high computational complexity Therefore techniques that enable efficient processing of deep neural networks to improve key metrics such as energy efficiency throughput and latency without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems The book includes background on DNN processing a description and taxonomy of hardware architectural approaches for designing DNN accelerators key metrics for evaluating and comparing different designs features of DNN processing that are amenable to hardware algorithm co design to improve energy efficiency and throughput and opportunities for applying new technologies Readers will find a structured introduction to the field as well as formalization and organization of key concepts from contemporary work that provide insights that may spark new ideas

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