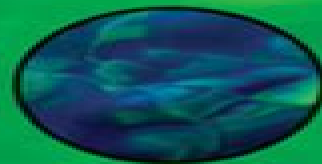


EMBEDDED
SoPC DESIGN WITH
NIOS II PROCESSOR AND
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PONG P. CHU

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Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor Embedded SoPC Design with Nios II Processor and Verilog Examples takes a learn by doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board Emphasizing hardware design and integration throughout the book is divided into four major parts Part I covers HDL and synthesis of custom hardware Part II introduces the Nios II processor and provides an overview of embedded software development Part III demonstrates the design and development of hardware and software of several complex I O peripherals including a PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides several case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology While designing and developing an embedded SoPC can be rewarding the learning can be a long and winding journey This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology

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adapted by other prototyping boards as long as a board has similar I O configuration

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fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology The book utilizes FPGA devices Nios II soft core processor and development platform from Altera Co which is one of the two main FPGA manufactures Altera has a generous university program that provides free software and discounted prototyping boards for educational institutions details at <http://www.altera.com/university> The two main educational prototyping boards are known as DE1-99 and DE2-69 All experiments can be implemented and tested with these boards A board combined with this book becomes a turn key solution for the SoPC design experiments and projects Most HDL and C codes in the book are device independent and can be adapted by other prototyping boards as long as a board has similar I/O configuration

Rapid Prototyping of Digital Systems James O. Hamblen, Tyson S. Hall, Michael D. Furman, 2007-10-31 Here is a laboratory workbook filled with interesting and challenging projects for digital logic design and embedded systems classes The workbook introduces you to fully integrated modern CAD tools logic simulation logic synthesis using hardware description languages design hierarchy current generation field programmable gate array technology and SoPC design Projects cover such areas as serial communications state machines with video output video games and graphics robotics pipelined RISC processor cores and designing computer systems using a commercial processor core

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Embedded Core Design with FPGAs Zainalabedin Navabi, 2007 This volume shows how a processor can be designed from scratch and by use of new EDA tools how it interfaces with its software It shows how a processor and its software can be used as an embedded core and used for the design of an embedded system

Rapid Prototyping of Digital Systems James O. Hamblen, Tyson S. Hall, Michael D. Furman, 2007-09-26 Here is a laboratory workbook filled with interesting and challenging projects for digital logic design and embedded systems classes The workbook introduces you to fully integrated modern CAD tools logic simulation logic synthesis using hardware description languages design hierarchy current generation field programmable gate array technology and SoPC design Projects cover such areas as serial communications state machines with video output video games and graphics robotics pipelined RISC processor cores and designing computer systems using a commercial processor core

Rapid Prototyping of Digital Systems James O. Hamblen, Tyson S. Hall, Michael D. Furman, 2006-01-16 Rapid Prototyping of Digital Systems Quartus II Edition provides an exciting and challenging laboratory component for undergraduate digital logic and computer design courses using FPGAs and CAD tools for simulation and hardware implementation The more advanced topics and exercises also make this text useful for upper level courses in digital logic programmable logic and embedded systems This new version of the widely used Rapid Prototyping of Digital Systems Second Edition now uses Altera's new Quartus II CAD tool and includes laboratory projects for Altera's UP 2 and the new UP 3 FPGA board Rapid Prototyping of Digital Systems

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Soft Core Processor Using Fpga Sangita Pokale,2013 This book present an application study in data logging device The new kind of soft core processor was designed based on NIOS II technology The device make use of NIOS II processor provided by ALT ERA to be implemented in FPGA NIOS II is a versatile embedded processor family that presents high performance and has been created for FPGA Author targets implementation NIOS II soft core processor from Altera FPGA Platform Also one of the FPGA vendor XILINX are providing Micro Blaze Pico Blaze RISC architecture This is of 32 bit processing architecture Author has implemented one simple digital circuit design on implementation of 8 bit asynchronous counter along with multiplexed seven segments LED Display Driver For HDL based circuit design Xilinx synthesis tool version 9 1 was used Also after having success in this implementation author has implemented NIOSII soft core processor using QuartusII 10 1 SOPC Builder Tool from Altera It reduces the hardware without changing the design by using SOPC approach It will definitely help the people who are having the field interest in FPGA ALTERA and NIOS II

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Embedded Sopc Design With Nios Ii Processor And Verilog Examples Book Review: Unveiling the Power of Words

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