DESIGN *of* COST-EFFICIENT INTERCONNECT PROCESSING UNITS

Spidergon STNoC

Marcello Coppola
Miltos D. Grammatikakis
Riccardo Locatelli
Giuseppe Maruccia
Lorenzo Pieralisi

Foreword by William Dally

Design Of Cost Efficient Interconnect Processing Units Spidergon Stnoc

Michael Hübner,Jürgen Becker

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Design of Cost-Efficient Interconnect Processing Units Marcello Coppola,Miltos D. Grammatikakis,Riccardo Locatelli,Giuseppe Maruccia,Lorenzo Pieralisi,2018-10-03 Streamlined Design Solutions Specifically for NoC To solve critical network on chip NoC architecture and design problems related to structure performance and modularity engineers generally rely on guidance from the abundance of literature about better understood system level interconnection networks However on chip networks present several distinct challenges that require novel and specialized solutions not found in the tried and true system level techniques A Balanced Analysis of NoC Architecture As the first detailed description of the commercial Spidergon STNoC architecture Design of Cost Efficient Interconnect Processing Units Spidergon STNoC examines the highly regarded cost cutting technology that is set to replace well known shared bus architectures such as STBus for demanding multiprocessor system on chip SoC applications Employing a balanced well organized structure simple teaching methods numerous illustrations and easy to understand examples the authors explain how the SoC and NoC technology works why developers designed it the way they did the system level design methodology and tools used to configure the Spidergon STNoC architecture differences in cost structure between NoCs and system level networks From professionals in computer sciences electrical engineering and other related fields to semiconductor vendors and investors all readers will appreciate the encyclopedic treatment of background NoC information ranging from CMPs to the basics of interconnection networks The text introduces innovative system level design methodology and tools for efficient design space exploration and topology selection It also provides a wealth of key theoretical and practical MPSoC and NoC topics such as technological deep sub micron effects homogeneous and heterogeneous processor architectures multicore SoC interconnect processing units generic NoC components and embeddings of common communication patterns **Design of Cost-Efficient Interconnect Processing Units** Marcello Coppola,Miltos D. Grammatikakis,Riccardo Locatelli,Giuseppe Maruccia,Lorenzo Pieralisi,2020-10-14 Streamlined Design Solutions Specifically for NoC To solve critical network on chip NoC architecture and design problems related to structure performance and modularity engineers generally rely on guidance from the abundance of literature about better understood system level interconnection networks However on chip networks present several distinct challenges that require novel and specialized solutions not found in the tried and true system level techniques A Balanced Analysis of NoC Architecture As the first detailed description of the commercial Spidergon STNoC architecture Design of Cost Efficient Interconnect Processing Units Spidergon STNoC examines the highly regarded cost cutting technology that is set to replace well known shared bus architectures such as STBus for demanding multiprocessor system on chip SoC applications Employing a balanced well organized structure simple teaching methods numerous illustrations and easy to understand examples the authors explain how the SoC and NoC technology works why developers designed it the way they did the system level design methodology and tools used to configure the Spidergon STNoC

architecture differences in cost structure between NoCs and system level networks From professionals in computer sciences electrical engineering and other related fields to semiconductor vendors and investors all readers will appreciate the encyclopedic treatment of background NoC information ranging from CMPs to the basics of interconnection networks The text introduces innovative system level design methodology and tools for efficient design space exploration and topology selection It also provides a wealth of key theoretical and practical MPSoC and NoC topics such as technological deep sub micron effects homogeneous and heterogeneous processor architectures multicore SoC interconnect processing units generic NoC components and embeddings of common communication patterns **VLSI 2010 Annual Symposium** Nikolaos Voros,Amar Mukherjee,Nicolas Sklavos,Konstantinos Masselos,Michael Huebner,2011-09-08 VLSI 2010 Annual Symposium will present extended versions of the best papers presented in ISVLSI 2010 conference The areas covered by the papers will include among others Emerging Trends in VLSI Nanoelectronics Molecular Biological and Quantum Computing MEMS VLSI Circuits and Systems Field programmable and Reconfigurable Systems System Level Design System on a Chip Design Application Specific Low Power VLSI System Design System Issues in Complexity Low Power Heat Dissipation Power Awareness in VLSI Design Test and Verification Mixed Signal Design and Analysis Electrical Packaging Co Design Physical Design Intellectual property creating and sharing **On-Chip Interconnect with aelite** Andreas Hansson,Kees Goossens,2010-10-20 The book provides a comprehensive description and implementation methodology for the Philips NXP Aethereal aelite Network on Chip NoC The presentation offers a systems perspective starting from the system requirements and deriving and describing the resulting hardware architectures embedded software and accompanying design flow Readers get an in depth view of the interconnect requirements not centered only on performance and scalability but also the multi faceted application driven requirements in particular composability and predictability The book shows how these qualitative requirements are implemented in a state of the art on chip interconnect and presents the realistic quantitative costs

Multi-Core Embedded Systems Georgios Kornaros,2018-10-08 Details a real world product that applies a cutting edge multi core architecture Increasingly demanding modern applications such as those used in telecommunications networking and real time processing of audio video and multimedia streams require multiple processors to achieve computational performance at the rate of a few giga operations per second This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores while being increasingly programmable blending processors and configurable hardware in a power efficient manner Multi Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous processors and heterogeneous multiple cores It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures as well as their limitations and potential for future growth Discusses the available programming models spread across different

abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system level parameters It addresses the use of existing open source and free tools originating from several application domains such as traffic modeling graph theory parallel computing and network simulation In addition the authors cover other important topics associated with multi core embedded systems such as Architectures and interconnects Embedded design methodologies Mapping of applications

On-Chip Networks Natalie Enright,Li-shiuan Peh,2022-11-10 With the ability to integrate a large number of cores on a single chip research into on chip networks to facilitate communication becomes increasingly important On chip networks seek to provide a scalable and high bandwidth communication substrate for multi core and many core architectures High bandwidth and low latency within the on chip network must be achieved while fitting within tight area and power budgets In this lecture we examine various fundamental aspects of on chip network design and provide the reader with an overview of the current state of the art research in this field Table of Contents Introduction Interface with System Architecture Topology Routing Flow Control Router Microarchitecture Conclusions *Routing Algorithms in Networks-on-Chip* Maurizio Palesi,Masoud Daneshtalab,2013-10-22 This book provides a single source reference to routing algorithms for Networks on Chip NoCs as well as in depth discussions of advanced solutions applied to current and next generation many core NoC based Systems on Chip SoCs After a basic introduction to the NoC design paradigm and architectures routing algorithms for NoC architectures are presented and discussed at all abstraction levels from the algorithmic level to actual implementation Coverage emphasizes the role played by the routing algorithm and is organized around key problems affecting current and next generation many core SoCs A selection of routing algorithms is included specifically designed to address key issues faced by designers in the ultra deep sub micron UDSM era including performance improvement power energy and thermal issues fault tolerance and reliability **Solutions on Embedded Systems** Massimo Conti,Simone Orcioni,Natividad Martínez Madrid,Ralf E.D. Seepold,2011-04-11 Embedded systems have an increasing importance in our everyday lives The growing complexity of embedded systems and the emerging trend to interconnections between them lead to new challenges Intelligent solutions are necessary to overcome these challenges and to provide reliable and secure systems to the customer under a strict time and financial budget Solutions on Embedded Systems documents results of several innovative approaches that provide intelligent solutions in embedded systems The objective is to present mature approaches to provide detailed information on the implementation and to discuss the results obtained *Designing 2D and 3D Network-on-Chip Architectures* Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies

are used to illuminate new design methodologies   Multiprocessor System-on-Chip Michael Hübner,Jürgen Becker,2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design   Embedded Artificial Intelligence Ovidiu Vermesan,Mario Diaz Nava,Björn Debaillie,2023-05-05 Recent technological developments in sensors edge computing connectivity and artificial intelligence AI technologies have accelerated the integration of data analysis based on embedded AI capabilities into resource constrained energy efficient hardware devices for processing information at the network edge Embedded AI combines embedded machine learning ML and deep learning DL based on neural networks NN architectures such as convolutional NN CNN or spiking neural network SNN and algorithms on edge devices and implements edge computing capabilities that enable data processing and analysis without optimised connectivity and integration allowing users to access data from various sources Embedded AI efficiently implements edge computing and AI processes on resource constrained devices to mitigate downtime and service latency and it successfully merges AI processes as a pivotal component in edge computing and embedded system devices Embedded AI also enables users to reduce costs communication and processing time by assembling data and by supporting user requirements without the need for continuous interaction with physical locations This book provides an overview of the latest research results and activities in industrial embedded AI technologies and applications based on close cooperation between three large scale ECSEL JU projects AI4DI ANDANTE and TEMPO The book s content targets researchers designers developers academics post graduate students and practitioners seeking recent research on embedded AI It combines the latest developments in embedded AI addressing methodologies tools and techniques to offer insight into technological trends and their use across different industries   Components and Services for IoT Platforms Georgios Keramidas,Nikolaos Voros,Michael Hübner,2016-09-23 This book serves as a single source reference to the state of the art in Internet of Things IoT platforms services tools programming languages and applications In particular the authors focus on IoT related requirements such as low power time to market connectivity reliability interoperability security and privacy Authors discuss the question of whether we need new IoT standardization bodies or initiatives toward a fully connected cyber physical world Coverage includes the research outcomes of several current European projects related to IoT platforms services APIs tools and applications   **Artificial Intelligence for Digitising Industry – Applications** Ovidiu Vermesan,2022-09-01 This book provides in depth insights into use cases implementing artificial intelligence AI applications at the edge It covers new ideas concepts research and innovation to enable the development and deployment of AI the industrial internet of things IIoT edge computing and digital twin technologies in industrial environments The work is based on the research results and activities of the AI4DI project

including an overview of industrial use cases research technological innovation validation and deployment This book s sections build on the research development and innovative ideas elaborated for applications in five industries automotive semiconductor industrial machinery food and beverage and transportation The articles included under each of these five industrial sectors discuss AI based methods techniques models algorithms and supporting technologies such as IIoT edge computing digital twins collaborative robots silicon born AI circuit concepts neuromorphic architectures and augmented intelligence that are anticipating the development of Industry 5 0 Automotive applications cover use cases addressing AI based solutions for inbound logistics and assembly process optimisation autonomous reconfigurable battery systems virtual AI training platforms for robot learning autonomous mobile robotic agents and predictive maintenance for machines on the level of a digital twin AI based technologies and applications in the semiconductor manufacturing industry address use cases related to AI based failure modes and effects analysis assistants neural networks for predicting critical 3D dimensions in MEMS inertial sensors machine vision systems developed in the wafer inspection production line semiconductor wafer fault classifications automatic inspection of scanning electron microscope cross section images for technology verification anomaly detection on wire bond process trace data and optical inspection The use cases presented for machinery and industrial equipment industry applications cover topics related to wood machinery with the perception of the surrounding environment and intelligent robot applications AI IIoT and robotics solutions are highlighted for the food and beverage industry presenting use cases addressing novel AI based environmental monitoring autonomous environment aware quality control systems for Champagne production and production process optimisation and predictive maintenance for soybeans manufacturing For the transportation sector the use cases presented cover the mobility as a service development of AI based fleet management for supporting multimodal transport This book highlights the significant technological challenges that AI application developments in industrial sectors are facing presenting several research challenges and open issues that should guide future development for evolution towards an environment friendly Industry 5 0 The challenges presented for AI based applications in industrial environments include issues related to complexity multidisciplinary and heterogeneity convergence of AI with other technologies energy consumption and efficiency knowledge acquisition reasoning with limited data fusion of heterogeneous data availability of reliable data sets verification validation and testing for decision making processes

Encyclopedia of Information Science and Technology, Third Edition Khosrow-Pour, D.B.A., Mehdi,2014-07-31 This 10 volume compilation of authoritative research based articles contributed by thousands of researchers and experts from all over the world emphasized modern issues and the presentation of potential opportunities prospective solutions and future directions in the field of information science and technology Provided by publisher   *Interconnect-Centric Design for Advanced SOC and NOC* Jari Nurmi,2004-07-20 In Interconnect centric Design for Advanced SoC and NoC we have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on

different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications   Power-efficient Design of On-chip Interconnection Networks Hangsheng Wang,2005

      Building Efficient, Reconfigurable Hardware Using Hierarchical Interconnects Chengcheng Wang,2013 In the semiconductor industry today ASICs are able to offer 10x 1000x higher energy and area efficiencies than non dedicated chips such as programmable DSP processers field programmable gate arrays FPGAs and microprocessors Not surprisingly SoCs today have become an integration of many ASIC blocks each performing a few dedicated tasks The growing size of modern SoC chips accelerated by the increasing demands for functionalities has exposed the major drawback of ASIC design cost These large SoCs are re designed a few times a year to rectify hardware bugs and to support new features Because ASICs are not reconfigurable even the smallest hardware change would require a re design Additionally design cost is rising exponentially with every technology generation The rising design cost of ASICs has exposed a huge need today efficiency and flexibility must co exist But among flexible hardware candidates microprocessors and programmable DSP processors are far too slow to meet the throughput requirements of ASICs FPGAs do come close in terms of performance but are extremely inefficient due to its high energy and large area overhead We must bridge the huge gap in efficiency for FPGA to become a viable contender to ASICs The primary culprit for FPGA inefficiency is interconnect which accounts for over 75% of area and delay For over 20 years 2D mesh network has been the back bone of FPGA interconnects but full connectivity in a 2D mesh require O N2 switches requiring interconnects to grow much faster than Moore s Law As a result various heuristics are used to simplify switch box arrays at the cost of resource utilization but interconnect area of modern FPGA is still around 80% This work builds FPGA using hierarchical interconnects based on Bene networks requiring O N log N switches Although Bene is commonly used in telecommunication this work is its first silicon realization of a FPGA To realize a highly efficient interconnect architecture significant pruning of the network is required Novel techniques such as fast path U turns and

unbalanced branching are also implemented A custom place and route software is developed to map benchmark designs on a variety of interconnect candidates From mapping results the architecture is updated based on network utilization until an optimized design is converged The large area of FPGA chip requires aggressive power gating PG but interconnect signals often lack spatial locality make it block level PG difficult A novel PG circuit technique is developed to power gate individual interconnect switches with very small overhead in area and performance Such technique requires fundamental circuit changes even modifying the CMOS inverter With innovations in chip architecture circuit design and extensive software development this work has demonstrated 5 user mappable FPGAs from 1K 16K LUTs all with around 50% interconnect area a 3 4x reduction from commercial FPGAs while preserving connectivity An energy efficiency of 1 1 GOPS mW is the highest among reported FPGAs and is 22x more efficient than the most efficient commercial FPGA today significantly bridging the efficiency gap between FPGA and ASIC

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