



# Download Time Domain Converters Voltage Controlled Oscillators Processing



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*Time-domain Analog-to-Digital Converters using Voltage-Controlled Oscillators* SeongHwan Cho,Jaewook Kim,Wonsik Yu,Young-Gyu Yoon,2015-06-24 This book describes time domain analog to digital converters ADCs using voltage controlled oscillators VCOs Unlike conventional ADCs that require precise analog circuits in the voltage domain time domain ADCs use mostly digital circuits that benefit from transistor scaling and therefore are suitable for current and future CMOS processes This book is intended for designers who want to build ADCs with advanced CMOS processes using digital building blocks

*VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters* Samantha Yoder,Mohammed Ismail,Waleed Khalil,2011-08-30 This book introduces the concept of voltage controlled oscillator VCO based analog to digital converters ADCs Detailed explanation is given of this promising new class of high resolution and low power ADCs which use time quantization as opposed to traditional analog based i e voltage ADCs *Linearizing Techniques for Voltage Controlled Oscillator Based Analog to Digital Converters* Sachin B. Rao,2013 Voltage controlled oscillator VCO based ADC is an important class of time domain ADC that has gained widespread acceptance due to their several desirable properties VCO based ADCs behave like an open loop continuous time delta sigma modulator and achieve excellent resolution by first order noise shaping the quantization error However the SNDR of an open loop VCO based ADC is severely distortion limited by the voltage to frequency tuning characteristics of the VCO This work examines various techniques that have already been proposed to overcome the VCO tuning non linearity problem Two new VCO based ADC architectures that overcome the limitations of the conventional approaches are proposed In the first approach the ADC is linearized by forcing the VCO to operate at only two operating points using a front end two level modulator With this technique the linearity is improved without using either a multi bit feedback DAC or calibration Fabricated in a 90 nm CMOS process the prototype ADC achieves better than 71 dB SFDR and 59.1 dB SNDR in 8 MHz signal bandwidth while consuming 4.3 mW power The ADC achieves a figure of merit of 366 fJ/conv step which is comparable with other state of the art time based ADCs In the second approach the need for a front end two level modulator is obviated using linearizers which introduce an inverse of VCO's voltage to frequency characteristics in the signal path A deterministic digital calibration unit runs continuously in the background and builds the inverse voltage to frequency transfer function Implemented in a 90nm CMOS process this on chip calibration improves SFDR of the prototype ADC from 46 dB to more than 83 dB The ADC consumes 4.1 mW power and achieves 73.9 dB SNDR in 5 MHz signal bandwidth resulting in an excellent figure of merit of 101 fJ/conv step

**Integrated Voltage Controlled Oscillators Using Large Time Constant Distributed Parameter Phase Shift Networks** Hans Helmut Stellrecht,1968 *Wide-Bandwidth High Dynamic Range D/A Converters* Konstantinos Doris,Arthur H.M. van Roermund,Domine Leenaerts,2006-01-12 IGH SPEED Digital to Analog D A converters are essential components in digital communication systems providing the necessary conversion of signals encoding information in bits to signals

encoding information in their amplitude vs time domain characteristics In general they are parts of a larger system the interface which consists of several signal conditioning circuits Dependent on where the converter is located within the chain of circuits in the interface signal processing operations are partitioned in those realized with digital techniques and those with analog The rapid evolution of CMOS technology has established implicit and explicit trends related to the interface and in particular to the D A converter The implicit relationship comes via the growth of digital systems First it is a global trend with respect to all interface circuits that increasing operating frequencies of digital systems place a similar demand for the interface circuits The second trend takes place locally within the interface Initially the D A converter was placed at the beginning of the interface chain and all signal conditioning was implemented in the analog domain after the D A conversion The increasing flexibility and robustness of digital signal processing shifted the D A converter closer to the end point of the chain where the demands for high quality high frequency operation are very high

**Voltage to Frequency Converter for Integration in Time Domain Induced Polarization Receiver** David G. Kissinger, 1977 *Voltage-controlled Oscillators*

Brian Partridge, 1978 We describe a simple software mimic of an analog to digital A D converter that is suitable for most laboratory applications requiring A D The routine samples output from a voltage controlled oscillator that can be built for around 6 Results of proving trials show the output to be linear and sampling rates of up to 50 sec are possible

**Power Efficient Analog-to-digital Converters Using Both Voltage and Time Domain Information** Taehwan Oh, 2013 As advanced wired and wireless communication systems attempt to achieve higher performance the demand for high resolution and wide signal bandwidth in their associated ADCs is strongly increased Recently time domain quantization has drawn attention from its scalability in deep submicron CMOS processes Furthermore there are several interesting aspects of time domain quantizer by processing the signal in time rather than only in voltage domain especially for power efficiency This research focuses on developing a new architecture for power efficient high resolution ADCs using both voltage and time domain information As a first approach a new delta sigma ADC based on a noise shaped two step integrating quantizer which quantizes the signal in voltage and time domains is presented Attaining an extra order of noise shaping from the integrating quantizer the proposed delta sigma ADC manifests a second order noise shaping with a first order loop filter Furthermore this quantizer provides an 8b quantization in itself drastically reducing the oversampling requirement The proposed ADC also incorporates a new feedback DAC topology that alleviates the feedback DAC complexity of a two step 8b quantizer The measured results of the prototype ADC implemented in a 0.13  $\mu\text{m}$  CMOS demonstrate peak SNDR of 70.7 dB 11.5 b ENOB at 8.1 mW power with an 8x OSR at 80 MHz sampling frequency To further improve ADC performance a Nyquist ADC based on a time based pipelined TDC is also proposed as a second approach In this work a simple V T conversion scheme with a cheap low gain amplifier in its first stage and a hybrid time domain quantization stage based on simple charge pump and capacitive DAC in its backend stages are also proposed to improve ADC linearity and power efficiency Using voltage and

time domain information the proposed ADC architecture is beneficial for both resolution and power efficiency with MSBs resolved in voltage domain and LSBs in time domain The measured results of the prototype ADC implemented in a 0.13  $\mu\text{m}$  CMOS demonstrate peak SNDR of 69.3 dB, 11.2 b ENOB at 6.38 mW power and 70 MHz sampling frequency The FOM is 38.2 fJ/conversion step

**Time-interleaved Analog-to-Digital Converters** Simon Louwsma, Ed van Tuijl, Bram Nauta, 2010-09-08 Time interleaved Analog to Digital Converters describes the research performed on low power time interleaved ADCs A detailed theoretical analysis is made of the time interleaved Track Hold since it must be capable of handling signals in the GHz range with little distortion and minimal power consumption Timing calibration is not attractive therefore design techniques are presented which do not require timing calibration The design of power efficient sub ADCs is addressed with a theoretical analysis of a successive approximation converter and a pipeline converter It turns out that the first can consume about 10 times less power than the latter and this conclusion is supported by literature Time interleaved Analog to Digital Converters describes the design of a high performance time interleaved ADC with much attention for practical design aspects aiming at both industry and research Measurements show best inclass performance with a sample rate of 1.8 GS/s, 7.9 ENOBs and a power efficiency of 1 pJ/conversion step

*Amplifier-based Analog-to-digital Converters Using Time-domain Signal Processing* [10], 2015

**Design of a Voltage-to-time Converter and Selection of a Time-to-digital Converter for Use in a Time-based Analog-to-digital Converter** Peter A. Osheroff, 2015

Efficient Use of Time Information in Analog-to-digital Converters Yue Hu, 2014 Time domain data conversion has recently drawn increased research attention for its highly digital nature in favor of process technology scaling Also as the time information being carried by binary voltage time domain operation is much less sensitive to voltage noise compared to conventional voltage domain operation However for analog to digital converter ADC application the challenge lies in the methodology of benefiting from time domain operation while maintaining improving the overall data conversion accuracy and power efficiency This dissertation has a focus on the investigation of novel data conversion topologies based on classic voltage domain operation that is capable of generating time information to improve ADC resolution system stability and speed without power penalty In the first approach a novel continuous time CT delta sigma modulator DSM using a time interleaved quantizer is proposed and implemented Along with the doubled sample rate the proposed architecture utilizes time information to perform correlated coupling between the two quantizer channels A 120 MS/s CT delta sigma ADC using proposed technique is implemented in 0.18  $\mu\text{m}$  CMOS process The measurement results achieve second order noise coupling from the interleaved quantizer itself without extra phases More importantly excess loop delay of two full sample clocks is compensated by time domain signal coupling the resulted CT DSM is fully stabilized in 120 MHz sampling rate and achieves 11 effective number of bits ENOB In the second approach a new category of pulse width modulation PWM scheme is proposed and described time symmetric PWM TSPWM An ADC structure is further proposed and implemented utilizing this

novel voltage to time converter followed by a first order noise shaped switched ring oscillator SRO TDC quantizer This ADC topology takes advantage of the TDC speed scaling for its digitized operation to boost the overall ADC resolution and signal bandwidth while the voltage to time front end is able to remain at a much lower speed than the TDC thanks to the proposed technique This is the first work that decouples the PWM modulation rate from TDC quantizing speed without distortion penalty Built in 0.18  $\mu\text{m}$  the implemented ADC is able to sample at a range from 20MHz to 40MHz the generated pulse train is quantized by the following SRO TDC at a rate of 400MHz The prototype chip shows a SFDR improvement over 24dB on the ADC output when TSPWM is used

#### **Millimeter-wave Voltage-controlled Oscillators and Frequency Doubler**

Yu-Ju Chuang, 2004

## **Download Time Domain Converters Voltage Controlled Oscillators Processing** Book Review: Unveiling the Magic of Language

In a digital era where connections and knowledge reign supreme, the enchanting power of language has be more apparent than ever. Its ability to stir emotions, provoke thought, and instigate transformation is really remarkable. This extraordinary book, aptly titled "**Download Time Domain Converters Voltage Controlled Oscillators Processing**," compiled by a very acclaimed author, immerses readers in a captivating exploration of the significance of language and its profound impact on our existence. Throughout this critique, we shall delve in to the book is central themes, evaluate its unique writing style, and assess its overall influence on its readership.

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