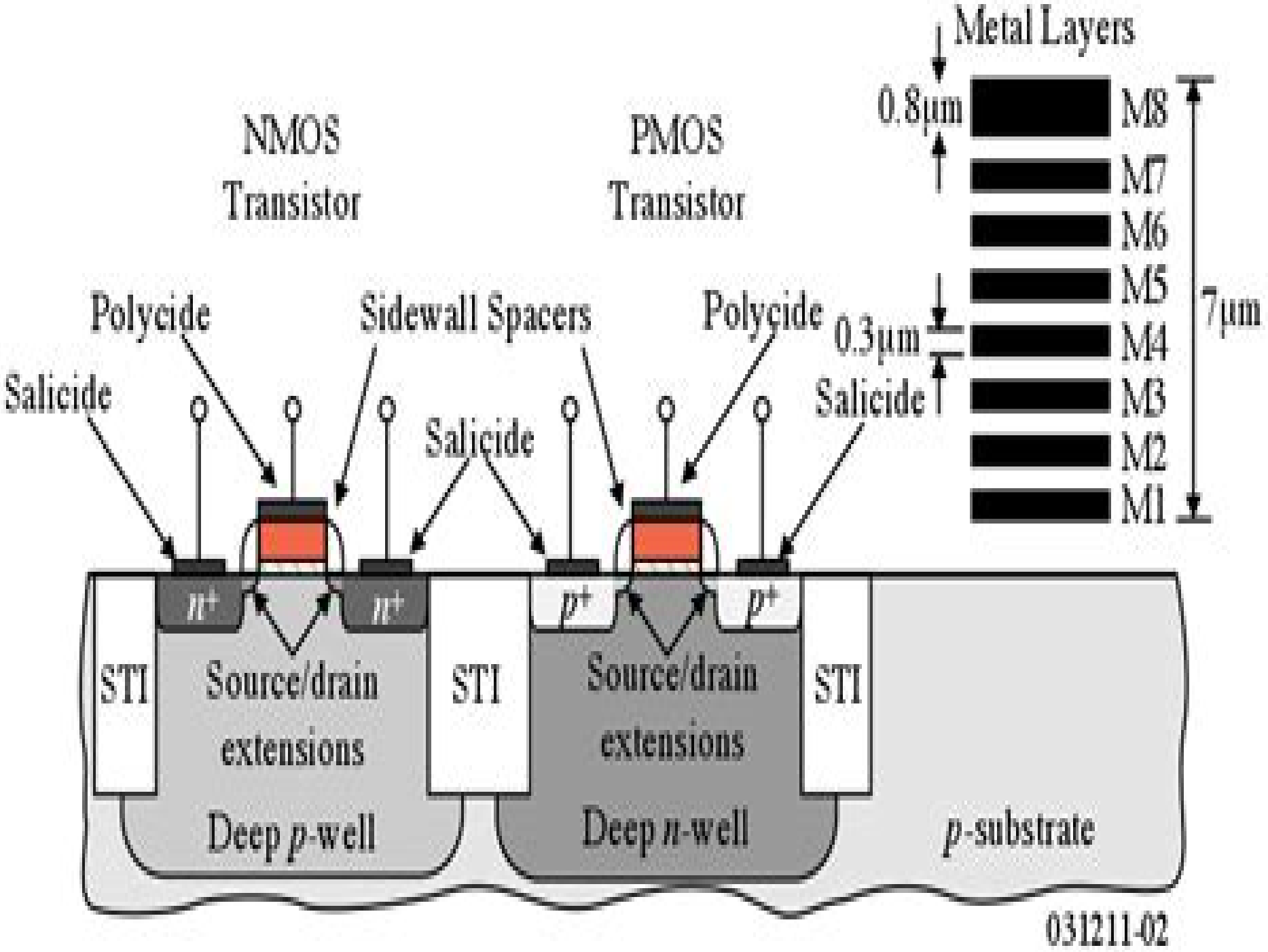
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Computational Scaling Technology For Deep Submicron Design

Svetlana N. Yanushkevich,Vlad P. Shmerko,Sergey Edward Lyshevski

Computational Scaling Technology For Deep Submicron Design:

Computational Scaling Technology for Deep Submicron Design Kafai Lai,2015-09-15 An understanding of computational scaling technology CST is essential for researchers and professionals involved in semiconductor design The first book to thoroughly explain CST this work provides ideas and directions for fully integrating design and technology within the field Focusing on modeling and simulations in computational lithography and design constraint optimization the book discusses the latest developments in design for manufacturing along with related design methods and challenges Examples of real world design technology co optimization DTCO test cases will help readers master the technology

Proceedings of the Second International Conference on Computational Intelligence and Informatics Vikrant Bhateja,João Manuel R.S. Tavares,B. Padmaja Rani,V. Kamakshi Prasad,K. Srujan Raju,2018-07-23 The volume contains 69 high quality papers presented at International Conference on Computational Intelligence and Informatics ICCII 2017 The conference was held during 25 27 September 2017 at Department of Computer Science and Engineering JNTUHCEH Hyderabad Telangana India This volume contains papers mainly focused on data mining wireless sensor networks parallel computing image processing network security MANETS natural language processing and internet of things Low Power Design in Deep Submicron Electronics W. Nebel,Jean Mermet,2013-06-29 Low Power Design in Deep Submicron Electronics deals with the different aspects of low power design for deep submicron electronics at all levels of abstraction from system level to circuit level and technology Its objective is to guide industrial and academic engineers and researchers in the selection of methods technologies and tools and to provide a baseline for further developments Furthermore the book has been written to serve as a textbook for postgraduate student courses In order to achieve both goals it is structured into different chapters each of which addresses a different phase of the design a particular level of abstraction a unique design style or technology These design related chapters are amended by motivations in Chapter 2 which presents visions both of future low power applications and technology advancements and by some advanced case studies in Chapter 9 From the Foreword This global nature of design for low power was well understood by Wolfgang Nebel and Jean Mermet when organizing the NATO workshop which is the origin of the book They invited the best experts in the field to cover all aspects of low power design As a result the chapters in this book are covering deep submicron CMOS digital system design for low power in a systematic way from process technology all the way up to software design and embedded software systems Low Power Design in Deep Submicron Electronics is an excellent guide for the practicing engineer the researcher and the student interested in this crucial aspect of actual CMOS design It contains about a thousand references to all aspects of the recent five years of feverish activity in this exciting aspect of design Hugo de Man Professor K U Leuven Belgium Senior Research Fellow IMEC Belgium Computational Intelligence in Digital and Network Designs and Applications Mourad Fakhfakh,Esteban Tlelo-Cuautle,Patrick Siarry,2015-07-14 This book explains the application of recent advances in computational intelligence

algorithms design methodologies and synthesis techniques to the design of integrated circuits and systems It highlights new biasing and sizing approaches and optimization techniques and their application to the design of high performance digital VLSI radio frequency and mixed signal circuits and systems This second of two related volumes addresses digital and network designs and applications with 12 chapters grouped into parts on digital circuit design network optimization and applications It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits **Networks on Chip** Axel Jantsch,Hannu Tenhunen,2007-05-08 As the number of processor cores and IP blocks integrated on a single chip is steadily growing a systematic approach to design the communication infrastructure becomes necessary Different variants of packed switched on chip networks have been proposed by several groups during the past two years This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces It also provides a guideline and vision about the direction this field is moving to Moreover the book outlines the consequences of adopting design platforms based on packet switched network The consequences may in fact be far reaching because many of the topics of distributed systems distributed real time systems fault tolerant systems parallel computer architecture parallel programming as well as traditional system on chip issues will appear relevant but within the constraints of a single chip VLSI implementation **VLSI and Chip Design** Dr. M. Maheswaran,Mandadupu Anusha,Bandam Narendar,Modugu Rambabu,2024-05-23 VLSI and Chip Design exploration of Very Large Scale Integration VLSI technology and the intricacies of modern chip design It fundamental principles advanced methodologies and the latest innovations in circuit design fabrication and testing With a focus on digital and analog systems this integrates theoretical concepts with practical applications catering to both beginners and professionals It emphasizes design optimization power efficiency and scalability making it an essential resource for engineers researchers and students aspiring to excel in semiconductor technology and integrated circuit design International Conference on Intelligent Computing and Smart Communication 2019 Geetam Singh Tomar,Narendra S. Chaudhari,Jorge Luis V. Barbosa,Mahesh Kumar Aghwariya,2020-01-07 This book gathers high quality research papers presented at the First International Conference ICSC 2019 organised by THDC Institute of Hydropower Engineering and Technology Tehri India from 20 to 21 April 2019 The book is divided into two major sections Intelligent Computing and Smart Communication Some of the areas covered are Parallel and Distributed Systems Web Services Databases and Data Mining Applications Feature Selection and Feature Extraction High Performance Data Mining Algorithms Knowledge Discovery Communication Protocols and Architectures High speed Communication High Voltage Insulation Technologies Fault Detection and Protection Power System Analysis Embedded Systems Architectures Electronics in Renewable Energy CAD for VLSI Green Electronics Signal and Image Processing Pattern Recognition and Analysis Multi Resolution Analysis and Wavelets 3D and Stereo Imaging and Neural Networks Photonic Interconnects for Computing

Systems Gabriela Nicolescu,Mahdi Nikdast,Sébastien Le Beux,2022-09-01 In recent years there has been a considerable amount of effort both in industry and academia focusing on the design implementation performance analysis evaluation and prediction of silicon photonic interconnects for inter and intra chip communication paving the way for the design and dimensioning of the next and future generation of high performance computing systems Photonic Interconnects for Computing Systems provides a comprehensive overview of the current state of the art technology and research achievements in employing silicon photonics for interconnection networks and high performance computing summarizing main opportunities and some challenges The majority of the chapters were collected from presentations made at the International Workshop on Optical Photonic Interconnects for Computing Systems OPTICS held over the past two years The workshop invites internationally recognized speakers on the range of topics relevant to silicon photonics and computing systems Technical topics discussed in the book include Design and Implementation of Chip Scale Photonic Interconnects Developing Design Automation Solutions for Chip Scale Photonic Interconnects Design Space Exploration in Chip Scale Photonic Interconnects Thermal Analysis and Modeling in Photonic Interconnects Design for Reliability Fabrication Non Uniformity in Photonic Interconnects Photonic Interconnects for Computing Systems presents a compilation of outstanding contributions from leading research groups in the field It presents a comprehensive overview of the design advantages challenges and requirements of photonic interconnects for computing systems The selected contributions present important discussions and approaches related to the design and development of novel photonic interconnect architectures as well as various design solutions to improve the performance of such systems while considering different challenges The book is ideal for personnel in computer photonic industries as well as academic staff and master graduate students in computer science and engineering electronic engineering electrical engineering and photonics *Built-in Fault-Tolerant Computing Paradigm for Resilient Large-Scale Chip Design* Xiaowei Li,Guihai Yan,Cheng Liu,2023-03-01 With the end of Dennard scaling and Moore s law IC chips especially large scale ones now face more reliability challenges and reliability has become one of the mainstay merits of VLSI designs In this context this book presents a built in on chip fault tolerant computing paradigm that seeks to combine fault detection fault diagnosis and error recovery in large scale VLSI design in a unified manner so as to minimize resource overhead and performance penalties Following this computing paradigm we propose a holistic solution based on three key components self test self diagnosis and self repair or 3S for short We then explore the use of 3S for general IC designs general purpose processors network on chip NoC and deep learning accelerators and present prototypes to demonstrate how 3S responds to in field silicon degradation and recovery under various runtime faults caused by aging process variations or radical particles Moreover we demonstrate that 3S not only offers a powerful backbone for various on chip fault tolerant designs and implementations but also has farther reaching implications such as maintaining graceful performance degradation mitigating the impact of verification blind spots and improving chip yield This book is the outcome of extensive

fault tolerant computing research pursued at the State Key Lab of Processors Institute of Computing Technology Chinese Academy of Sciences over the past decade The proposed built in on chip fault tolerant computing paradigm has been verified in a broad range of scenarios from small processors in satellite computers to large processors in HPCs Hopefully it will provide an alternative yet effective solution to the growing reliability challenges for large scale VLSI designs **IBM Journal of Research and Development** ,2003 High Performance Computing for Big Data Chao Wang,2017-10-16 High Performance Computing for Big Data Methodologies and Applications explores emerging high performance architectures for data intensive applications novel efficient analytical strategies to boost data processing and cutting edge applications in diverse fields such as machine learning life science neural networks and neuromorphic engineering The book is organized into two main sections The first section covers Big Data architectures including cloud computing systems and heterogeneous accelerators It also covers emerging 3D IC design principles for memory architectures and devices The second section of the book illustrates emerging and practical applications of Big Data across several domains including bioinformatics deep learning and neuromorphic engineering Features Covers a wide range of Big Data architectures including distributed systems like Hadoop Spark Includes accelerator based approaches for big data applications such as GPU based acceleration techniques and hardware acceleration such as FPGA CGRA ASICs Presents emerging memory architectures and devices such as NVM STT RAM 3D IC design principles Describes advanced algorithms for different big data application domains Illustrates novel analytics techniques for Big Data applications scheduling mapping and partitioning methodologies Featuring contributions from leading experts this book presents state of the art research on the methodologies and applications of high performance computing for big data applications About the Editor Dr Chao Wang is an Associate Professor in the School of Computer Science at the University of Science and Technology of China He is the Associate Editor of ACM Transactions on Design Automations for Electronics Systems TODAES Applied Soft Computing Microprocessors and Microsystems IET Computers Digital Techniques and International Journal of Electronics Dr Chao Wang was the recipient of Youth Innovation Promotion Association CAS ACM China Rising Star Honorable Mention 2016 and best IP nomination of DATE 2015 He is now on the CCF Technical Committee on Computer Architecture CCF Task Force on Formal Methods He is a Senior Member of IEEE Senior Member of CCF and a Senior Member of ACM *Scientific Computing in Electrical Engineering* Wilhelmus H. Schilders,E. Jan W. ter Maten,Stephan H. M. J. Houben,2013-11-27 **Neural Information Processing and VLSI** Bing J. Sheu,Joongho Choi,2012-12-06 Neural Information Processing and VLSI provides a unified treatment of this important subject for use in classrooms industry and research laboratories in order to develop advanced artificial and biologically inspired neural networks using compact analog and digital VLSI parallel processing techniques Neural Information Processing and VLSI systematically presents various neural network paradigms computing architectures and the associated electronic optical implementations using efficient VLSI design methodologies Conventional digital machines cannot perform

computationally intensive tasks with satisfactory performance in such areas as intelligent perception including visual and auditory signal processing recognition understanding and logical reasoning where the human being and even a small living animal can do a superb job Recent research advances in artificial and biological neural networks have established an important foundation for high performance information processing with more efficient use of computing resources The secret lies in the design optimization at various levels of computing and communication of intelligent machines Each neural network system consists of massively paralleled and distributed signal processors with every processor performing very simple operations thus consuming little power Large computational capabilities of these systems in the range of some hundred giga to several tera operations per second are derived from collectively parallel processing and efficient data routing through well structured interconnection networks Deep submicron very large scale integration VLSI technologies can integrate tens of millions of transistors in a single silicon chip for complex signal processing and information manipulation The book is suitable for those interested in efficient neurocomputing as well as those curious about neural network system applications It has beenespecially prepared for use as a text for advanced undergraduate and first year graduate students and is an excellent reference book for researchers and scientists working in the fields covered *Embedded and Ubiquitous Computing* Laurence T. Yang,Minyi Guo,Guang R. Gao,Niraj K. Jha,2004-07-30 Welcome to the proceedings of the 2004 International Conference on Embedded and Ubiquitous Computing EUC 2004 which was held in Aizu Wakamatsu City Japan 25 27 August 2004 Embedded and ubiquitous computing are emerging rapidly as exciting new paradigms and disciplines to provide computing and communication services all the time everywhere Its systems are now invading every aspect of life to the point that they are disappearing inside all sorts of appliances or can be worn unobtrusively as part of clothing and jewelry etc This emergence is a natural outcome of research and technological advances in embedded systems pervasive computing and communications wireless networks mobile computing distri ted computing and agent technologies etc Its explosive impact on academia industry government and daily life can be compared to that of electric motors over the past century but promises to revolutionize life much more profoundly than elevators electric motors or even personal computer evolution ever did The EUC 2004 conference provided a forum for engineers and scientists in academia industry and government to address all the resulting profound ch lenges including technical safety social legal political and economic issues and to present and discuss their ideas results work in progress and experience on all aspects of embedded and ubiquitous computing There was a very large number of paper submissions 260 from more than 20countriesandregions includingnotonlyAsiaandthePaci c butalsoEurope and North America All submissions were reviewed by at least three program or technical committee members or external reviewers *Coevolutionary Computation and Multiagent Systems* Li-cheng Jiao,Jing Liu,Weicai Zhong,2012 The origins of evolutionary computation can be traced back to the late 1950 s where it remained almost unknown to the broader scientific community for three decades until the 1980 s when it started to receive significant attention as did the study of

multi agent systems MAS This focuses on systems in which many intelligent agents interact with each other Today these systems are not simply a research topic but are also beginning to become an important subject of academic teaching and industrial and commercial application Co Evolutionary Computational and Multi Agent Systems introduces the author s recent work in these two new and important branches of artificial intelligence High Performance Computing - HiPC 2008 P. Sadayappan,Manish Parashar,Ramamurthy Badrinath,Viktor K. Prasanna,2008-12-17 This book constitutes the refereed proceedings of the 15th International Conference on High Performance Computing HiPC 2008 held in Bangalore India in December 2008 The 46 revised full papers presented together with the abstracts of 5 keynote talks were carefully reviewed and selected from 317 submissions The papers are organized in topical sections on applications performance optimizazion parallel algorithms and applications scheduling and resource management sensor networks energy aware computing distributed algorithms communication networks as well as architecture **Soft Computing and Industry** Rajkumar Roy,Mario Köppen,Seppo Ovaska,Takeshi Furuhashi,Frank Hoffmann,2012-12-06 Soft computing embraces various methodologies for the development of intelligent systems that have been successfully applied to a large number of real world problems Soft Computing in Industry contains a collection of papers that were presented at the 6th On line World Conference on Soft Computing in Industrial Applications that was held in September 2001 It provides a comprehensive overview of recent theoretical developments in soft computing as well as of successful industrial applications It is divided into seven parts covering material on keynote papers on various subjects ranging from computing with autopoietic systems to the effects of the Internet on education intelligent control classification clustering and optimization image and signal processing agents multimedia and Internet theoretical advances prediction design and diagnosis The book is aimed at researchers and professional engineers who develop and apply intelligent systems in computer engineering **International Conference on Innovative Computing and Communications** Ashish Khanna,Deepak Gupta,Siddhartha Bhattacharyya,Vaclav Snasel,Jan Platos,Aboul Ella Hassanien,2019-11-16 This book gathers high quality research papers presented at the Second International Conference on Innovative Computing and Communication ICICC 2019 which was held at the VSB Technical University of Ostrava Czech Republic on 21 22 March 2019 Highlighting innovative papers by scientists scholars students and industry experts in the fields of computing and communication the book promotes the transformation of fundamental research into institutional and industrialized research and the translation of applied research into real world applications

Smart Intelligent Computing and Communication Technology V.D. Ambeth Kumar,S. Malathi,V.E. Balas,2021-10-07 Recent developments in the fields of intelligent computing and communication have paved the way for the handling of current and upcoming problems and brought about significant technological advancements This book presents the proceedings of IConIC 2021 the 4th International Conference on Intelligent Computing held on 26 and 27 March 2021 in Chennai India The principle objective of the annual IConIC conference is to provide an international scientific forum where

participants can exchange innovative ideas in relevant fields and interact in depth through discussion with their peer group The theme of the 2021 conference and this book is Smart Intelligent Computing and Communication Technology and the 109 papers included here focus on the technological innovations and trendsetting initiatives in medicine industry education and security that are improving and optimizing business and technical processes and enabling inclusive growth The papers are grouped under 2 headings Evolution of Computing Intelligence and Computing and Communication and cover a broad range of intelligent computing research and applications The book provides an overview of the cutting edge developments and emerging areas of study in the technological fields of intelligent computing and will be of interest to researchers and practitioners from both academia and industry **Logic Design of NanoICS** Svetlana N. Yanushkevich,Vlad P. Shmerko,Sergey Edward Lyshevski,2017-12-19 Today s engineers will confront the challenge of a new computing paradigm relying on micro and nanoscale devices Logic Design of NanoICs builds a foundation for logic in nanodimensions and guides you in the design and analysis of nanoICs using CAD The authors present data structures developed toward applications rather than a purely theoretical treatment Requiring only basic logic and circuits background Logic Design of NanoICs draws connections between traditional approaches to design and modern design in nanodimensions The book begins with an introduction to the directions and basic methodology of logic design at the nanoscale then proceeds to nanotechnologies and CAD graphical representation of switching functions and networks word level and linear word level data structures 3 D topologies based on hypercubes multilevel circuit design and fault tolerant computation in hypercube like structures The authors propose design solutions and techniques going beyond the underlying technology to provide more applied knowledge This design oriented reference is written for engineers interested in developing the next generation of integrated circuitry illustrating the discussion with approximately 250 figures and tables 100 equations 250 practical examples and 100 problems Each chapter concludes with a summary references and a suggested reading section

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