

Chapter 2 Solutions

Case Study 1: Optimizing Cache Performance via Advanced Techniques

- 2.1
 - a. Each element is 8B. Since a 64B cacheline has 8 elements, and each column access will result in fetching a new line for the non-ideal matrix, we need a minimum of 8×8 (64 elements) for each matrix. Hence, the minimum cache size is $128 \times 8\text{B} = 1\text{KB}$.
 - b. The blocked version only has to fetch each input and output element once. The unblocked version will have one cache miss for every $64\text{B}/8\text{B} = 8$ row elements. Each column requires $64\text{B} \times 256$ of storage, or 16KB. Thus, column elements will be replaced in the cache before they can be used again. Hence the unblocked version will have 9 misses (1 row and 8 columns) for every 2 in the blocked version.
 - c.


```

for (i = 0; i < 256; i=i+8) {
    for (j = 0; j < 256; j=j+8) {
        for(m=0; m<8; m++) {
            for(n=0; n<8; n++) {
                output[j+n][i+m] = input[i+m][j+n];
            }
        }
    }
}
          
```
 - d. 2-way set associative. In a direct-mapped cache the blocks could be allocated so that they map to overlapping regions in the cache.
 - e. You should be able to determine the level-1 cache size by varying the block size. The ratio of the blocked and unblocked program speeds for arrays that do not fit in the cache in comparison to blocks that do is a function of the cache block size, whether the machine has out-of-order issue, and the bandwidth provided by the level-2 cache. You may have discrepancies if your machine has a write-through level-1 cache and the write buffer becomes a limiter of performance.
- 2.2 Since the unblocked version is too large to fit in the cache, processing eight 8B elements requires fetching one 64B row cache block and 8 column cache blocks. Since each iteration requires 2 cycles without misses, prefetches can be initiated every 2 cycles, and the number of prefetches per iteration is more than one, the memory system will be completely saturated with prefetches. Because the latency of a prefetch is 16 cycles, and one will start every 2 cycles, $16/2 = 8$ will be outstanding at a time.
- 2.3 Open hands-on exercise, no fixed solution.

Computer Architecture Quantitative Approach Solution Instructor Manual

Shasha Hu



Computer Architecture Quantitative Approach Solution Instructor Manual:

Computer Architecture John L. Hennessy, David A. Patterson, 2002-05-29 This best selling title considered for over a decade to be essential reading for every serious student and practitioner of computer design has been updated throughout to address the most important trends facing computer designers today In this edition the authors bring their trademark method of quantitative analysis not only to high performance desktop machine design but also to the design of embedded and server systems They have illustrated their principles with designs from all three of these domains including examples from consumer electronics multimedia and web technologies and high performance computing The book retains its highly rated features Fallacies and Pitfalls which share the hard won lessons of real designers Historical Perspectives which provide a deeper look at computer design history Putting it all Together which present a design example that illustrates the principles of the chapter Worked Examples which challenge the reader to apply the concepts theories and methods in smaller scale problems and Cross Cutting Issues which show how the ideas covered in one chapter interact with those presented in others In addition a new feature Another View presents brief design examples in one of the three domains other than the one chosen for Putting It All Together The authors present a new organization of the material as well reducing the overlap with their other text Computer Organization and Design A Hardware Software Approach 2 e and offering more in depth treatment of advanced topics in multithreading instruction level parallelism VLIW architectures memory hierarchies storage devices and network technologies Also new to this edition is the adoption of the MIPS 64 as the instruction set architecture In addition to several online appendixes two new appendixes will be printed in the book one contains a complete review of the basic concepts of pipelining the other provides solutions a selection of the exercises Both will be invaluable to the student or professional learning on her own or in the classroom Hennessy and Patterson continue to focus on fundamental techniques for designing real machines and for maximizing their cost performance Presents state of the art design examples including IA 64 architecture and its first implementation the Itanium Pipeline designs for Pentium III and Pentium IV The cluster that runs the Google search engine EMC storage systems and their performance Sony Playstation 2 Infiniband a new storage area and system area network SunFire 6800 multiprocessor server and its processor the UltraSPARC III Trimedia TM32 media processor and the Transmeta Crusoe processor Examines quantitative performance analysis in the commercial server market and the embedded market as well as the traditional desktop market Updates all the examples and figures with the most recent benchmarks such as SPEC 2000 Expands coverage of instruction sets to include descriptions of digital signal processors media processors and multimedia extensions to desktop processors Analyzes capacity cost and performance of disks over two decades Surveys the role of clusters in scientific computing and commercial computing Presents a survey taxonomy and the benchmarks of errors and failures in computer systems Presents detailed descriptions of the design of storage systems and of clusters Surveys memory hierarchies in modern microprocessors and the key parameters of modern

disks Presents a glossary of networking terms □□□□□□□□□□/□□□□ John L. Hennessy,□□□□,David A. Patterson,1999

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system usage by focusing on the principles used in hardware systems design and the methods for enhancing performance

Architectures, Languages and Techniques for Concurrent Systems World Occam and Transputer User Group.

Technical Meeting, 1999 During the past fifteen years concurrency in programming languages such as Java rose and fell and again became popular At this moment developers advise us to avoid concurrency in programming They are using a host of deprecated methods in the latest releases How are we to understand the love hate relationship with what should be a widely used approach of tackling real world problems The aim of architectures Languages and Techniques is to encourage the safe efficient and effective use of parallel computing It is generally agreed that concurrency is found in most real applications and that it should be natural to use concurrency in programming However there has grown up a myth that concurrency is hard and only for the hardened expert The papers collected in this book cover the whole spectrum of concurrency from theoretical underpinnings to applications The message passing style of concurrency developed in the Communicating Sequential Processes CSP approach is considered and extensions are proposed CSP's realization in the programming language occam is used directly for applications as diverse as modeling of concurrent systems and the description of concurrent hardware This latter application may be compared to the use of Java for the same purpose Concurrency and the use of Java is the subject of further papers as is the provision of CSP like facilities in Java and C and techniques to use these languages to construct reliable concurrent systems At a time when concurrency gives headaches this book brings a welcome breath of fresh air Concurrency can really be a positive way forward

Computer Organization, Design, and Architecture, Fifth Edition

Sajjan G. Shiva, 2013-12-20 Suitable for a one or two semester undergraduate or beginning graduate course in computer science and computer engineering Computer Organization Design and Architecture Fifth Edition presents the operating principles capabilities and limitations of digital computers to enable the development of complex yet efficient systems With 11 new sections and four revised sections this edition takes students through a solid up to date exploration of single and multiple processor systems embedded architectures and performance evaluation See What's New in the Fifth Edition Expanded coverage of embedded systems mobile processors and cloud computing Material for the Architecture and Organization part of the 2013 IEEE ACM Draft Curricula for Computer Science and Engineering Updated commercial machine architecture examples The backbone of the book is a description of the complete design of a simple but complete hypothetical computer The author then details the architectural features of contemporary computer systems selected from Intel MIPS ARM Motorola Cray and various microcontrollers etc as enhancements to the structure of the simple computer He also introduces performance enhancements and advanced architectures including networks distributed systems GRIDs and cloud computing Computer organization deals with providing just enough details on the operation of the computer system for sophisticated users and programmers Often books on digital systems architecture fall into four categories logic design computer organization hardware design and system architecture This book captures the important attributes of these four

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