

CHAPTER 1 INTRODUCTION

- 1.1** An ADD/SUBTRACT logic circuit is shown below. It performs the ADD operation for $P = 0$, and SUBTRACT for $P = 1$.
- Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for transmission gate and XOR, are inverting. For example, AND gate is implemented with NAND followed by an inverter.
 - By using the gate array platform given on page 47, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.



Figure P14.1(a)

SOLUTION:

- The CMOS circuit implementation using the gate array platform:

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Integrated Circuits Charles F. Wojslaw, 1978 Digital integrated Circuits, 1976 **Instructor's Manual for Digital Integrated Circuit Design** Ken Martin, 2000 This manual is a gratis item to be given to instructors who have adopted Digital Integrated Circuit Design by Ken Martin This manual contains complete solutions prepared by the author to all of the exercises in the text *Device Electronics for Integrated Circuits* Richard S. Muller, Theodore I. Kamins, K. C. Hsieh, J. H. Kim, B. Y. Liu, 1986 *Solution Manual Digital Logic* Jefferson C. Boyce, 1982 **Digital Integrated Circuits** Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolić, 2008 *Digital Integrated Circuits*, **Integrated Electronics** Jacob Millman, 1972 Digital Integrated Circuits Jan M. Rabaey, 2003 *Digital Integrated Circuits Manual* Jack Cazes, 1975

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