

Bernhard Goll  
Horst Zimmermann

# Comparators in Nanometer CMOS Technology



Springer

# Comparators In Nanometer Cmos Technology Springer Series In Advanced Microelectronics

**S Baum**



## **Comparators In Nanometer Cmos Technology Springer Series In Advanced Microelectronics:**

Comparators in Nanometer CMOS Technology Bernhard Goll, Horst Zimmermann, 2014-09-15 This book covers the complete spectrum of the fundamentals of clocked regenerative comparators their state of the art advanced CMOS technologies innovative comparators inclusive circuit aspects their characterization and properties Starting from the basics of comparators and the transistor characteristics in nanometer CMOS seven high performance comparators developed by the authors in 120nm and 65nm CMOS are described extensively Methods and measurement circuits for the characterization of advanced comparators are introduced A synthesis of the largely differing aspects of demands on modern comparators and the properties of devices being available in nanometer CMOS which are posed by the so called nanometer hell of physics is accomplished The book summarizes the state of the art in integrated comparators Advanced measurement circuits for characterization will be introduced as well as the method of characterization by bit error analysis usually being used for characterization of optical receivers The book is compact and the graphical quality of the illustrations is outstanding This book is written for engineers and researchers in industry as well as scientists and Ph D students at universities It is also recommendable to graduate students specializing on nanoelectronics and microelectronics or circuit design *Delta-Sigma A/D-Converters* Richard Gaggli, 2012-12-17 The emphasis of this book is on practical design aspects for broadband A D converters for communication systems The embedded designs are employed for transceivers in the field of ADSL solutions and WLAN applications An area and power efficient realization of a converter is mandatory to remain competitive in the market The right choice for the converter topology and architecture needs to be done very carefully to result in a competitive FOM The book begins with a brief overview of basic concepts about ADSL and WLAN to understand the ADC requirements At architectural level issues on different modulator topologies are discussed employing the provided technology node The design issues are pointed out in detail for modern digital CMOS technologies beginning with 180nm followed by 130nm and going down to 65nm feature size Beside practical aspects challenges to mixed signal design level are addressed to optimize the converters in terms of consumed chip area power consumption and design for high yield in volume production Thus careful considerations on circuit and architectural level are performed by introducing a dynamic biasing technique a feed forward approach and a resolution in time instead of amplitude resolution **Advanced Informatics for Computing**

**Research** Ashish Kumar Luhach, Dharm Singh Jat, Uttam Ghosh, Xiao-Zhi Gao, Pawan Lingras, 2025-03-28 This two volume set constitutes the revised selected papers of the 6th International Conference on Advanced Informatics for Computing Research ICAICR 2023 held in Rohtak Haryana India in December 16 17 2023 The 58 full papers presented in these proceedings were carefully reviewed and selected from 225 submissions They are organized in topical sections as follows Volume number 2072 Artificial Intelligence Data Science Human computer interaction HCI Machine Learning Volume number 2073 Machine Learning Security and Privacy **Optoelectronic Circuits in Nanometer CMOS Technology** Mohamed Atef, Horst

Zimmermann,2016-03-04 This book describes the newest implementations of integrated photodiodes fabricated in nanometer standard CMOS technologies It also includes the required fundamentals the state of the art and the design of high performance laser drivers transimpedance amplifiers equalizers and limiting amplifiers fabricated in nanometer CMOS technologies This book shows the newest results for the performance of integrated optical receivers laser drivers modulator drivers and optical sensors in nanometer standard CMOS technologies Nanometer CMOS technologies rapidly advanced enabling the implementation of integrated optical receivers for high data rates of several Giga bits per second and of high pixel count optical imagers and sensors In particular low cost silicon CMOS optoelectronic integrated circuits became very attractive because they can be extensively applied to short distance optical communications such as local area network chip to chip and board to board interconnects as well as to imaging and medical sensors      **Silicon Optoelectronic Integrated Circuits**

Horst Zimmermann,2019-01-30 This book reviews various topics in optoelectronics and the design of microelectronic circuits It introduces readers to the essential features of optical absorption and device physics of photodetectors as well as their integration in modern CMOS and BiCMOS technologies This information provides the basis for understanding the underlying mechanisms of Optoelectronic Integrated Circuits OEICs which are described in the main part of the book In the second edition of this book new and outstanding integrated high bandwidth pin photodiodes as well as avalanche photodiodes in the linear mode and in the Geiger mode are introduced To cover the topic comprehensively the book presents detailed descriptions of OEICs for a wide range of applications from various optical sensors smart sensors image sensors 3D sensors and optical storage systems to fiber receivers and receivers for optical wireless communication as well as single photon detection This new edition also reflects the latest trends in OEIC research on integrated optical receivers at the quantum limit and electronic photonic integration and highlights outstanding 3D integrated application examples like a multi node optical switch an optical transceiver and a high resolution 3D sensor      **Variation Aware**

**Analog and Mixed-Signal Circuit Design in Emerging Multi-Gate CMOS Technologies** Michael Fulde,2009-10-27 Since scaling of CMOS is reaching the nanometer area serious limitations enforce the introduction of novel materials device architectures and device concepts Multi gate devices employing high k gate dielectrics are considered as promising solution overcoming these scaling limitations of conventional planar bulk CMOS Variation Aware Analog and Mixed Signal Circuit Design in Emerging Multi Gate CMOS Technologies provides a technology oriented assessment of analog and mixed signal circuits in emerging high k and multi gate CMOS technologies      *Low-Power High-Speed ADCs for Nanometer CMOS*

*Integration* Zhiheng Cao,Shouli Yan,2008-07-08 Low Power High Speed ADCs for Nanometer CMOS Integration is about the design and implementation of ADC in nanometer CMOS processes that achieve lower power consumption for a given speed and resolution than previous designs through architectural and circuit innovations that take advantage of unique features of nanometer CMOS processes A phase lock loop PLL clock multiplier has also been designed using new circuit techniques and

successfully tested 1 A 1 2V 52mW 210MS s 10 bit two step ADC in 130nm CMOS occupying 0.38mm<sup>2</sup> Using offset canceling comparators and capacitor networks implemented with small value interconnect capacitors to replace resistor ladder multiplexer in conventional sub ranging ADCs it achieves 74dB SFDR for 10MHz and 71dB SFDR for 100MHz input 2 A 32mW 1 25GS s 6 bit ADC with 2.5GHz internal clock in 130nm CMOS A new type of architecture that combines flash and SAR enables the lowest power consumption 6 bit 1GS s ADC reported to date This design can be a drop in replacement for existing flash ADCs since it does not require any post processing or calibration step and has the same latency as flash 3 A 0.4ps rms jitter integrated from 3kHz to 300MHz offset for 2.5GHz 1 3GHz tunable phase noise programmable clock multiplier PLL for generating sampling clock to the SAR ADC A new loop filter structure enables phase error preamplification to lower PLL in band noise without increasing loop filter capacitor size

*Nanometer CMOS RFICs for Mobile TV Applications* Ahmed A. Youssef, James Haslett, 2010-06-17 Nanometer CMOS RFICs for Mobile TV Applications focuses on how to break the trade off between power consumption and performance linearity and noise figure by optimizing the mobile TV front end dynamic range in three hierarchical levels the intrinsic MOSFET level the circuit level and the architectural level It begins by discussing the fundamental concepts of MOSFET dynamic range including nonlinearity and noise It then moves to the circuit level introducing the challenges associated with designing wide dynamic range variable gain broadband low noise amplifiers LNAs The book gives a detailed analysis of a new noise canceling technique that helps CMOS LNAs achieve a sub 2 dB wideband noise figure Lastly the book deals with the front end dynamic range optimization process from the systems perspective by introducing the active and passive automatic gain control AGC mechanism

**Nanometer CMOS SIGMA-Delta Modulators for Software Defined Radio**, 2011-09-11

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