

Bo Fu · Paul Ampadu

# Error Control for Network-on-Chip Links

 Springer

# Error Control For Network On Chip Links

**Guillaume Favre**

A decorative red circular graphic with a gradient, appearing as a partial circle or a stylized 'C' shape, located to the right of the author's name.

## **Error Control For Network On Chip Links:**

*Error Control for Network-on-Chip Links* Bo Fu, Paul Ampadu, 2011-10-09 This book provides readers with a comprehensive review of the state of the art in error control for Network on Chip NOC links Coverage includes detailed description of key issues in NOC error control faced by circuit and system designers as well as practical error control techniques to minimize the impact of these errors on system performance

**Transient and Permanent Error Control for Networks-on-Chip** Qiaoyan Yu, Paul Ampadu, 2011-11-18 This book addresses reliability and energy efficiency of on chip networks using cooperative error control It describes an efficient way to construct an adaptive error control codec capable of tracking noise conditions and adjusting the error correction strength at runtime Methods are also presented to tackle joint transient and permanent error correction exploiting the redundant resources already available on chip A parallel and flexible network simulator is also introduced which facilitates examining the impact of various error control methods on network on chip performance

**Network-on-Chip** Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers

students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems      **Network-on-Chip Security and Privacy** Prabhat Mishra, Subodha Charles, 2021-05-03 This book provides comprehensive coverage of Network on Chip NoC security vulnerabilities and state of the art countermeasures with contributions from System on Chip SoC designers academic researchers and hardware security experts Readers will gain a clear understanding of the existing security solutions for on chip communication architectures and how they can be utilized effectively to design secure and trustworthy systems      **Reliability, Availability and Serviceability of**

**Networks-on-Chip** Érika Cota, Alexandre de Moraes Amory, Marcelo Soares Lubaszewski, 2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures

*Networks on Chips* Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs      Coding Theory Sudhakar Radhakrishnan, Muhammad Sarfraz, 2020-03-11 This book is intended to attract the attention of practitioners and researchers in academia and industry interested in challenging paradigms of coding theory and computer vision The chapters in this comprehensive reference explore the latest developments methods approaches and applications of coding theory in a wide variety of fields and endeavours This book is compiled with a view to provide researchers academicians and readers with an in depth discussion of the latest advances in this field It consists of twelve chapters from academicians practitioners and researchers from different disciplines of life All the chapters are authored by various researchers around the world covering the field of coding theory and image and video processing This book mainly focusses on researchers who can do quality research in the area of coding theory and image and video processing and related fields Each chapter is an independent research study which will motivate young researchers to think about These twelve chapters are presented in three sections and will be an eye opener for all who systematic researchers in these fields      Networks on Chip Axel Jantsch, Hannu Tenhunen, 2007-05-08 As the number of processor cores and IP blocks integrated on a single chip is steadily growing a systematic approach to design the

communication infrastructure becomes necessary. Different variants of packed switched on chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system on chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

*Architecture of Computing Systems -- ARCS 2016* Frank Hannig, João M.P. Cardoso, Thilo

Pionteck, Dietmar Fey, Wolfgang Schröder-Preikschat, Jürgen Teich, 2016-03-24. This book constitutes the proceedings of the 29th International Conference on Architecture of Computing Systems ARCS 2016 held in Nuremberg, Germany in April 2016. The 29 full papers presented in this volume were carefully reviewed and selected from 87 submissions. They were organized in topical sections named: configurable and in memory accelerators, network on chip and secure computing architectures, cache architectures and protocols, mapping of applications on heterogeneous architectures and real time tasks on multiprocessors, all about time, timing tracing and performance modeling, approximate and energy efficient computing, allocation from memories to FPGA hardware modules, organic computing systems and reliability aspects in NoCs, caches and GPUs.

**Design Technologies for Green and Sustainable Computing Systems** Partha Pratim Pande, Amlan

Ganguly, Krishnendu Chakrabarty, 2013-07-17. This book provides a comprehensive guide to the design of sustainable and green computing systems. GSC coverage includes important breakthroughs in various aspects of GSC including multi core architectures, interconnection technology, data centers, high performance computing, HPC and sensor networks. The authors address the challenges of power efficiency and sustainability in various contexts including system design, computer architecture, programming languages, compilers and networking.

**Reconfigurable Networks-on-Chip** Sao-Jie

Chen, Ying-Cherng Lan, Wen-Chung Tsai, Yu-Hen Hu, 2011-12-15. This book provides a comprehensive survey of recent progress in the design and implementation of Networks on Chip. It addresses a wide spectrum of on chip communication problems ranging from physical network to application layers. Specific topics that are explored in detail include packet routing, resource arbitration, error control, correction, application mapping and communication scheduling. Additionally, a novel bi directional communication channel NoC BiNoC architecture is described with detailed explanation. Written for practicing engineers in need of practical knowledge about the design and implementation of networks on chip. Includes tutorial like details to introduce readers to a diverse range of NoC designs as well as in depth analysis for designers with NoC experience to explore advanced issues. Describes a variety of on chip communication architectures including a novel bi directional communication channel NoC. From the Foreword. Overall, this book shows important advances over the state of the art that

will affect future system design as well as R D in tools and methods for NoC design It represents an important reference point for both designers and electronic design automation researchers and developers Giovanni De Micheli      **Network Algorithmics** George Varghese,Jun Xu,2022-11-11 Network Algorithmics An Interdisciplinary Approach to Designing Fast Networked Devices Second Edition takes an interdisciplinary approach to applying principles for efficient implementation of network devices offering solutions to the problem of network implementation bottlenecks In designing a network device there are dozens of decisions that affect the speed with which it will perform sometimes for better but sometimes for worse The book provides a complete and coherent methodology for maximizing speed while meeting network design goals The book is uniquely focused on the seamless integration of data structures algorithms operating systems and hardware software co designs for high performance routers switches and network end systems Thoroughly updated based on courses taught by the authors over the past decade the book lays out the bottlenecks most often encountered at four disparate levels of implementation protocol OS hardware and architecture It then develops fifteen principles key to breaking these bottlenecks systematically applying them to bottlenecks found in end nodes interconnect devices and specialty functions located along the network Later sections discuss the inherent challenges of modern cloud computing and data center networking Offers techniques that address common bottlenecks of interconnect devices including routers bridges gateways endnodes and Web servers Presents many practical algorithmic concepts that students and readers can work with immediately Revised and updated throughout to discuss the latest developments from authors courses including measurement algorithmics randomization regular expression matching and software defined networking Includes a new rich set of homework exercises and exam questions to facilitate classroom use      *Evolutionary Based Solutions for Green Computing* Samee Ullah Khan,Joanna Kołodziej,Juan Li,Albert Y. Zomaya,2012-08-14 Today s highly parameterized large scale distributed computing systems may be composed of a large number of various components computers databases etc and must provide a wide range of services The users of such systems located at different geographical or managerial network cluster may have a limited access to the system s services and resources and different often conflicting expectations and requirements Moreover the information and data processed in such dynamic environments may be incomplete imprecise fragmentary and overloading All of the above mentioned issues require some intelligent scalable methodologies for the management of the whole complex structure which unfortunately may increase the energy consumption of such systems An optimal energy utilization has reached to a point that many information technology IT managers and corporate executives are all up in arms to identify scalable solution that can reduce electricity consumption so that the total cost of operation is minimized of their respective large scale computing systems and simultaneously improve upon or maintain the current throughput of the system This book in its eight chapters addresses the fundamental issues related to the energy usage and the optimal low cost system design in high performance green computing systems The recent evolutionary and general metaheuristic based solutions for energy

optimization in data processing scheduling resource allocation and communication in modern computational grids could and network computing are presented along with several important conventional technologies to cover the hot topics from the fundamental theory of the green computing concept and to describe the basic architectures of systems This book points out the potential application areas and provides detailed examples of application case studies in low energy computational systems The development trends and open research issues are also outlined All of those technologies have formed the foundation for the green computing that we know of today

#### **Low-Power NoC for High-Performance SoC Design**

Hoi-Jun Yoo,Kangmin Lee,Jun Kyong Kim,2018-10-08 Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation Low Power NoC for High Performance SoC Design provides practical knowledge and real examples of how to use network on chip NoC in the design of system on chip SoC It discusses many architectural and theoretical studies on NoCs including design methodology topology exploration quality of service guarantee low power design and implementation trials The Steps to Implement NoC The book covers the full spectrum of the subject from theory to actual chip design using NoC Employing the Unified Modeling Language UML throughout it presents complicated concepts such as models of computation and communication computation partitioning in a manner accessible to laypeople The authors provide guidelines on how to simplify complex networking theory to design a working chip In addition they explore the novel NoC techniques and implementations of the Basic On Chip Network BONE project Examples of real time decisions circuit level design systems and chips give the material a real world context Low Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design this book shows how to build the complicated interconnections on SoC while keeping a low power consumption

#### **Design and Test Technology for Dependable Systems-on-Chip**

Ubar, Raimund,Raik, Jaan,Vierhaus, Heinrich Theodor,2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC

**Energy-Efficient Fault-Tolerant Systems** Jimson Mathew,Rishad A. Shafik,Dhiraj K. Pradhan,2013-09-07 This book describes the state of the art in energy efficient fault tolerant embedded systems It covers the entire product lifecycle of electronic systems design analysis and testing and includes discussion of both circuit and system level approaches Readers will be enabled to meet the conflicting design objectives of energy efficiency and fault tolerance for reliability given the up to date techniques presented

**'Advances in Microelectronics: Reviews', Vol\_1** Sergey Yurish,2017-12-24 The 1st volume of Advances in Microelectronics Reviews Book Series contains 19 chapters written by 72 authors from academia and industry from 16 countries With unique combination of information in each volume the Advances in Microelectronics Reviews Book Series will be of value for scientists and engineers in industry and at universities In order to offer a fast and easy reading of the state of the art of each topic every chapter in this book is independent and self contained All chapters have the same structure first

an introduction to specific topic under study second particular field description including sensing applications Each of chapter is ending by well selected list of references with books journals conference proceedings and web sites This book ensures that readers will stay at the cutting edge of the field and get the right and effective start point and road map for the further researches and developments

On-Chip Communication Architectures Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that will have a significant impact on research and design of communication architectures over the next several years

Design, Automation, and Test in Europe Rudy Lauwereins, Jan Madsen, 2008-01-08 In 2007 The Design Automation and Test in Europe DATE conference celebrated its tenth anniversary As a tribute to the chip and system level design and design technology community this book presents a compilation of the three most influential papers of each year This provides an excellent historical overview of the evolution of a domain that contributed substantially to the growth and competitiveness of the circuit electronics and systems industry

*Advances in Computers* Marvin Zelkowitz, 2005 The term computation gap has been defined as the difference between the computational power demanded by the application domain and the computational power of the underlying computer platform Traditionally closing the computation gap has been one of the major and fundamental tasks of computer architects However as technology advances and computers become more pervasive in the society the domain of computer architecture has been extended The scope of research in the computer architecture is no longer restricted to the computer hardware and organization issues A wide spectrum of topics ranging from algorithm design to power management is becoming part of the computer architecture Based on the aforementioned trend and to reflect recent research efforts attempts were made to select a collection of articles that covers different aspects of contemporary computer architecture design This volume of the *Advances in Computers*



contains six chapters on different aspects of computer architecture Key features Wide range of research topics Coverage of new topics such as power management Network on Chip Load balancing in distributed systems and pervasive computing Simple writing style Wide range of research topics Coverage of new topics such as power management Network on Chip Load balancing in distributed systems and pervasive computing Simple writing style

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