DESIGN *of* COST-EFFICIENT INTERCONNECT PROCESSING UNITS

Spidergon STNoC

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Design Of Cost Efficient Interconnect Processing Units Spidergon Stnoc System On Chip Design And Technologies

Georgios Keramidas,Nikolaos Voros,Michael Hübner

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Design of Cost-Efficient Interconnect Processing Units Marcello Coppola,Miltos D. Grammatikakis,Riccardo Locatelli,Giuseppe Maruccia,Lorenzo Pieralisi,2018-10-03 Streamlined Design Solutions Specifically for NoC To solve critical network on chip NoC architecture and design problems related to structure performance and modularity engineers generally rely on guidance from the abundance of literature about better understood system level interconnection networks However on chip networks present several distinct challenges that require novel and specialized solutions not found in the tried and true system level techniques A Balanced Analysis of NoC Architecture As the first detailed description of the commercial Spidergon STNoC architecture Design of Cost Efficient Interconnect Processing Units Spidergon STNoC examines the highly regarded cost cutting technology that is set to replace well known shared bus architectures such as STBus for demanding multiprocessor system on chip SoC applications Employing a balanced well organized structure simple teaching methods numerous illustrations and easy to understand examples the authors explain how the SoC and NoC technology works why developers designed it the way they did the system level design methodology and tools used to configure the Spidergon STNoC architecture differences in cost structure between NoCs and system level networks From professionals in computer sciences electrical engineering and other related fields to semiconductor vendors and investors all readers will appreciate the encyclopedic treatment of background NoC information ranging from CMPs to the basics of interconnection networks The text introduces innovative system level design methodology and tools for efficient design space exploration and topology selection It also provides a wealth of key theoretical and practical MPSoC and NoC topics such as technological deep sub micron effects homogeneous and heterogeneous processor architectures multicore SoC interconnect processing units generic NoC components and embeddings of common communication patterns   Design of Cost-Efficient Interconnect Processing Units Marcello Coppola,Miltos D. Grammatikakis,Riccardo Locatelli,Giuseppe Maruccia,Lorenzo Pieralisi,2020-10-14 Streamlined Design Solutions Specifically for NoC To solve critical network on chip NoC architecture and design problems related to structure performance and modularity engineers generally rely on guidance from the abundance of literature about better understood system level interconnection networks However on chip networks present several distinct challenges that require novel and specialized solutions not found in the tried and true system level techniques A Balanced Analysis of NoC Architecture As the first detailed description of the commercial Spidergon STNoC architecture Design of Cost Efficient Interconnect Processing Units Spidergon STNoC examines the highly regarded cost cutting technology that is set to replace well known shared bus architectures such as STBus for demanding multiprocessor system on chip SoC applications Employing a balanced well organized structure simple teaching methods numerous illustrations and easy to understand examples the authors explain how the SoC and NoC technology works why developers

designed it the way they did the system level design methodology and tools used to configure the Spidergon STNoC architecture differences in cost structure between NoCs and system level networks From professionals in computer sciences electrical engineering and other related fields to semiconductor vendors and investors all readers will appreciate the encyclopedic treatment of background NoC information ranging from CMPs to the basics of interconnection networks The text introduces innovative system level design methodology and tools for efficient design space exploration and topology selection It also provides a wealth of key theoretical and practical MPSoC and NoC topics such as technological deep sub micron effects homogeneous and heterogeneous processor architectures multicore SoC interconnect processing units generic NoC components and embeddings of common communication patterns **Embedded Artificial Intelligence** Ovidiu Vermesan,Mario Diaz Nava,Björn Debaillie,2023-05-05 Recent technological developments in sensors edge computing connectivity and artificial intelligence AI technologies have accelerated the integration of data analysis based on embedded AI capabilities into resource constrained energy efficient hardware devices for processing information at the network edge Embedded AI combines embedded machine learning ML and deep learning DL based on neural networks NN architectures such as convolutional NN CNN or spiking neural network SNN and algorithms on edge devices and implements edge computing capabilities that enable data processing and analysis without optimised connectivity and integration allowing users to access data from various sources Embedded AI efficiently implements edge computing and AI processes on resource constrained devices to mitigate downtime and service latency and it successfully merges AI processes as a pivotal component in edge computing and embedded system devices Embedded AI also enables users to reduce costs communication and processing time by assembling data and by supporting user requirements without the need for continuous interaction with physical locations This book provides an overview of the latest research results and activities in industrial embedded AI technologies and applications based on close cooperation between three large scale ECSEL JU projects AI4DI ANDANTE and TEMPO The book s content targets researchers designers developers academics post graduate students and practitioners seeking recent research on embedded AI It combines the latest developments in embedded AI addressing methodologies tools and techniques to offer insight into technological trends and their use across different industries **Artificial Intelligence for Digitising Industry Applications** Ovidiu Vermesan,2022-09-01 This book provides in depth insights into use cases implementing artificial intelligence AI applications at the edge It covers new ideas concepts research and innovation to enable the development and deployment of AI the industrial internet of things IIoT edge computing and digital twin technologies in industrial environments The work is based on the research results and activities of the AI4DI project including an overview of industrial use cases research technological innovation validation and deployment This book s sections build on the research development and innovative ideas elaborated for applications in five industries automotive semiconductor industrial machinery food and beverage and transportation The articles included under each of these five

industrial sectors discuss AI based methods techniques models algorithms and supporting technologies such as IIoT edge computing digital twins collaborative robots silicon born AI circuit concepts neuromorphic architectures and augmented intelligence that are anticipating the development of Industry 5 0 Automotive applications cover use cases addressing AI based solutions for inbound logistics and assembly process optimisation autonomous reconfigurable battery systems virtual AI training platforms for robot learning autonomous mobile robotic agents and predictive maintenance for machines on the level of a digital twin AI based technologies and applications in the semiconductor manufacturing industry address use cases related to AI based failure modes and effects analysis assistants neural networks for predicting critical 3D dimensions in MEMS inertial sensors machine vision systems developed in the wafer inspection production line semiconductor wafer fault classifications automatic inspection of scanning electron microscope cross section images for technology verification anomaly detection on wire bond process trace data and optical inspection The use cases presented for machinery and industrial equipment industry applications cover topics related to wood machinery with the perception of the surrounding environment and intelligent robot applications AI IIoT and robotics solutions are highlighted for the food and beverage industry presenting use cases addressing novel AI based environmental monitoring autonomous environment aware quality control systems for Champagne production and production process optimisation and predictive maintenance for soybeans manufacturing For the transportation sector the use cases presented cover the mobility as a service development of AI based fleet management for supporting multimodal transport This book highlights the significant technological challenges that AI application developments in industrial sectors are facing presenting several research challenges and open issues that should guide future development for evolution towards an environment friendly Industry 5 0 The challenges presented for AI based applications in industrial environments include issues related to complexity multidisciplinary and heterogeneity convergence of AI with other technologies energy consumption and efficiency knowledge acquisition reasoning with limited data fusion of heterogeneous data availability of reliable data sets verification validation and testing for decision making processes

Designing 2D and 3D Network-on-Chip Architectures Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Solutions on Embedded Systems Massimo Conti,Simone Orcioni,Natividad Martínez Madrid,Ralf E.D. Seepold,2011-04-11 Embedded systems have an increasing importance in our everyday lives The growing complexity of embedded systems and the emerging trend to interconnections between them lead to new challenges Intelligent solutions are necessary to overcome these challenges and to provide reliable and secure systems to the customer under a strict time and

financial budget Solutions on Embedded Systems documents results of several innovative approaches that provide intelligent solutions in embedded systems The objective is to present mature approaches to provide detailed information on the implementation and to discuss the results obtained **Multiprocessor System-on-Chip** Michael Hübner,Jürgen Becker,2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design *Encyclopedia of Information Science and Technology, Third Edition* Khosrow-Pour, D.B.A., Mehdi,2014-07-31 This 10 volume compilation of authoritative research based articles contributed by thousands of researchers and experts from all over the world emphasized modern issues and the presentation of potential opportunities prospective solutions and future directions in the field of information science and technology Provided by publisher **Components and Services for IoT Platforms** Georgios Keramidas,Nikolaos Voros,Michael Hübner,2016-09-23 This book serves as a single source reference to the state of the art in Internet of Things IoT platforms services tools programming languages and applications In particular the authors focus on IoT related requirements such as low power time to market connectivity reliability interoperability security and privacy Authors discuss the question of whether we need new IoT standardization bodies or initiatives toward a fully connected cyber physical world Coverage includes the research outcomes of several current European projects related to IoT platforms services APIs tools and applications *Interconnect-Centric Design for Advanced SOC and NOC* Jari Nurmi,2004-07-20 In Interconnect centric Design for Advanced SoC and NoC we have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications Program Management for System on Chip

Platforms Whitson G. Waldo,2010-09 A Fully Integrated Presentation of New Hardware and Software Product Introductions Using Program Management Methodologies for System on Chip Platforms If you re an executive manager or engineer in the semiconductor software or systems industries this book provides conceptual views ranging from the design of integrated circuits or systems on a chip through fabrication to integration of chips onto boards and through development of enablement and runtime software for system and platform deliveries Special features included this book are Program management methodologies General management fundamentals An overview of leadership principles Basic discrete device technology Internal structure and operation of some common logic gates Basic integrated circuit design concepts building blocks and flow Chip packaging technologies Details of the fabrication process for integrated circuits Printed circuit board design manufacture and test Software design development and test Integrated circuit test silicon validation and device qualification Program management applications bringing it all together The book explores interactions and dependencies of technologies that impact systems and platforms This is a valuable resource to learn these technologies or to use as a reference

Variation Tolerant On-Chip Interconnects Ethiopia Enideg Nigussie,2011-12-02 This book presents design techniques analysis and implementation of high performance and power efficient variation tolerant on chip interconnects Given the design paradigm shift to multi core interconnect centric designs and the increase in sources of variability and their impact in sub 100nm technologies this book will be an invaluable reference for anyone concerned with the design of next generation high performance electronics systems **On-Chip Communication Architectures** Sudeep Pasricha,Nikil Dutt,2010 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architecures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years Multicore Systems On-Chip: Practical Software/Hardware Design Abderazek Ben

Abdallah,2013-07-20 System on chips designs have evolved from fairly simple unicore single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon To meet high computational demands posed by latest consumer electronic devices most current systems are based on such paradigm which represents a real revolution in many aspects in computing The attraction of multicore processing for power reduction is compelling By splitting a set of tasks among multiple processor cores the operating frequency necessary for each core can be reduced allowing to reduce the voltage on each core Because dynamic power is proportional to the frequency and to the square of the voltage we get a big gain even though we may have more cores running As more and more cores are integrated into these designs to share the ever increasing processing load the main challenges lie in efficient memory hierarchy scalable system interconnect new programming paradigms and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility Current design methods tend toward mixed HW SW co designs targeting multicore systems on chip for specific applications To decide on the lowest cost mix of cores designers must iteratively map the device s functionality to a particular HW SW partition and target architectures In addition to connect the heterogeneous cores the architecture requires high performance complex communication architectures and efficient communication protocols such as hierarchical bus point to point connection or Network on Chip Software development also becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores especially heterogeneous cores is very difficult **System-on-Chip** Bashir M. Al-Hashimi,2006-01-31 This book highlights both the key achievements of electronic systems design targeting SoC implementation style and the future challenges presented by the continuing scaling of CMOS technology *An Experimental Investigation of an On-chip Interconnect Fabric Using a Multiprocessor System-on-chip Architecture* Priya Bangal,2011 Recent advances in technology have made it possible to integrate systems with CPUs memory units buses specialized logic other digital functions and their interconnections on a single chip giving rise to the concept of system on chip SoC architectures In order to keep up with the incoming data rates of modern applications and to handle concurrent real world events in real time multiprocessor SoC implementations have become necessary As more processors and peripherals are being integrated on a single chip providing an efficient and a functionally optimum interconnection has become a major design challenge The traditional shared bus based approach is quite popular in SoC architectures as it is simple well understood and easy to implement However its scalability is limited since the bus invariably becomes a bottleneck as more processors are added Switch based networks can overcome this bottleneck while providing true concurrency and task level parallelism resulting in a higher throughput However switch based networks are complex and consume considerable amounts of logic resources on a chip thus increasing

the cost Hence the choice of switch based networks over a bus based architecture is an important design consideration in SoC architectures This choice hinges on the trade off between design simplicity and low cost vs high communication bandwidth This research investigates the logic resource utilization of a switch based on chip interconnect to analyze its scalability for multiprocessor systems It also experimentally demonstrates the true concurrency provided by the interconnect investigates the arbitration mechanism used and suggests the use of a real time operating system RTOS as a more effective way of managing on chip interconnections **System-on-chip Design and Technologies** ,20?? Interconnect Technology and Design for Gigascale Integration Jeffrey A. Davis,James D. Meindl,2012-12-06 Interconnect Technology and Design for Gigascale Integration is the cumulative effort from academic researchers at Georgia Tech MIT and Stanford as well as from industry researchers at IBM T J Watson Research Center LSI Logic and SUN microsystems The material found in this book is unique in that it spans IC interconnect topics ranging from IBM s revolutionary copper process to an in depth exploration into interconnect aware computer architectures This broad swath of topics presented by leaders in the research field is intended to provide a comprehensive perspective on interconnect technology and design issues so that the reader will understand the implications of the semiconductor industry s next substantial milestone gigascale integration

System-on-Chip for Real-Time Applications Wael Badawy,Graham A. Julien,2002-10-31 System on Chip for Real Time Applications will be of interest to engineers both in industry and academia working in the area of SoC VLSI design and application It will also be useful to graduate and undergraduate students in electrical and computer engineering and computer science A selected set of papers from the 2nd International Workshop on Real Time Applications were used to form the basis of this book It is organized into the following chapters Introduction Design Reuse Modeling Architecture Design Techniques Memory Circuits Low Power Interconnect and Technology MEMS System on Chip for Real Time Applications contains many signal processing applications and will be of particular interest to those working in that community

Unique Chips and Systems Eugene John,Juan Rubio,2018-10-08 Which came first the system or the chip While integrated circuits enable technology for the modern information age computing communication and network chips fuel it As soon as the integration ability of modern semiconductor technology offers presents opportunities issues in power consumption reliability and form factor present challenges The demands of emerging software applications can only be met with unique systems and chips Drawing on contributors from academia research and industry Unique Systems and Chips explores unique approaches to designing future computing and communication chips and systems The book focuses on specialized hardware and systems as opposed to general purpose chips and systems It covers early conception and simulation mid development application testing and performance The chapter authors introduce new ideas and innovations in unique aspects of chips and system design then go on to provide in depth analysis of these ideas They explore ways in which these chips and systems may be used in further designs or products spurring innovations beyond the intended scopes of those presented International in

flavor the book brings industrial and academic perspectives into focus by presenting the full spectrum of applications of chips and systems

Design Of Cost Efficient Interconnect Processing Units Spidergon Stnoc System On Chip Design And Technologies Book Review: Unveiling the Magic of Language

In an electronic era where connections and knowledge reign supreme, the enchanting power of language has be apparent than ever. Its capability to stir emotions, provoke thought, and instigate transformation is really remarkable. This extraordinary book, aptly titled "**Design Of Cost Efficient Interconnect Processing Units Spidergon Stnoc System On Chip Design And Technologies**," published by a highly acclaimed author, immerses readers in a captivating exploration of the significance of language and its profound affect our existence. Throughout this critique, we shall delve into the book is central themes, evaluate its unique writing style, and assess its overall influence on its readership.

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