

FPGA-Based System Design

Wayne Wolf



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classical logic design techniques relate to FPGA based logic design Understanding FPGA fabrics the basic programmable structures of FPGAs Specifying and optimizing logic to address size speed and power consumption Verilog VHDL and software tools for optimizing logic and designs The structure of large digital systems including register transfer design methodology Building large scale platform and multi FPGA systems A start to finish DSP case study addressing a wide range of design problems PRENTICE HALL Professional Technical Reference Upper Saddle River NJ 07458 www.phptr.com ISBN 0 13 142461 0

Distributed Embedded Systems: Design, Middleware and Resources Bernd Kleinjohann, Lisa Kleinjohann, Marilyn Wolf, 2008-07-10 This year the IFIP Working Conference on Distributed and Parallel Embedded Systems DIPES 2008 is held as part of the IFIP World Computer Congress held in Milan on September 7 10 2008 The embedded systems world has a great deal of experience with parallel and distributed computing Many embedded computing systems require the high performance that can be delivered by parallel computing Parallel and distributed computing are often the only ways to deliver adequate real time performance at low power levels This year's conference attracted 30 submissions of which 21 were accepted Prof Jorg Henkel of the University of Karlsruhe graciously contributed a keynote address on embedded computing and reliability We would like to thank all of the program committee members for their diligence Wayne Wolf Bernd Kleinjohann and Lisa Kleinjohann Acknowledgements We would like to thank all people involved in the organization of the IFIP World Computer Congress 2008 especially the IPC Co Chairs Judith Bishop and Ivo De Lotto the Organization Chair Giulio Occhini as well as the Publications Chair John Impagliazzo Further thanks go to the authors for their valuable contributions to DIPES 2008 Last but not least we would like to acknowledge the considerable amount of work and enthusiasm spent by our colleague Claudius Stern in preparing the proceedings of DIPES 2008

Hemade it possible to produce them in their current professional and homogeneous style **Modern VLSI Design** Wayne Wolf, 2008-12-21 The Number 1 VLSI Design Guide Now Fully Updated for IP Based Design and the Newest Technologies Modern VLSI Design Fourth Edition offers authoritative up to the minute guidance for the entire VLSI design process from architecture and logic design through layout and packaging Wayne Wolf has systematically updated his award winning book for today's newest technologies and highest value design techniques Wolf introduces powerful new IP based design techniques at all three levels gates subsystems and architecture He presents deeper coverage of logic design fundamentals clocking and timing and much more No other VLSI guide presents as much up to date information for maximizing performance minimizing power utilization and achieving rapid design turnarounds Power Integrity Modeling and Design for Semiconductors and Systems Madhavan Swaminathan, Ege Engin, 2007-11-19 The First Comprehensive Example Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers package designers and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems Now for the first time there's a complete guide to power integrity modeling everything you need to know from

the basics through the state of the art Using realistic case studies and downloadable software examples two leading experts demonstrate today's best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise The authors carefully introduce the core concepts of power distribution design systematically present and compare leading techniques for modeling noise and link these techniques to specific applications Their many examples range from the simplest using analytical equations to compute power supply noise through complex system level applications The authors introduce power delivery network components analysis high frequency measurement and modeling requirements Thoroughly explain modeling of power ground planes including plane behavior lumped modeling distributed circuit based approaches and much more Offer in depth coverage of simultaneous switching noise including modeling for return currents using time and frequency domain analysis Introduce several leading time domain simulation methods such as macromodeling and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high speed servers high speed differential signaling chip package analysis materials characterization embedded decoupling capacitors and electromagnetic bandgap structures This book's system level focus and practical examples will make it indispensable for every student and professional concerned with power integrity including electrical engineers system designers signal integrity engineers and materials scientists It will also be valuable to developers building software that helps to analyze high speed systems

Signal and Power Integrity--simplified Eric Bogatin, 2010 With the inclusion of the two new hot topics in signal integrity power integrity and high speed serial links this book will be the most up to date complete guide to understanding and designing for signal integrity

Reconfigurable Computing Maya B. Gokhale, Paul S. Graham, 2006-07-04 A one of a kind survey of the field of Reconfigurable Computing Gives a comprehensive introduction to a discipline that offers a 10X 100X acceleration of algorithms over microprocessors Discusses the impact of reconfigurable hardware on a wide range of applications signal and image processing network security bioinformatics and supercomputing Includes the history of the field as well as recent advances Includes an extensive bibliography of primary sources

Timing Analysis and Simulation for Signal Integrity Engineers Greg Edlund, 2007-10-22 Every day companies call upon their signal integrity engineers to make difficult decisions about design constraints and timing margins Can I move these wires closer together How many holes can I drill in this net How far apart can I place these chips Each design is unique there's no single recipe that answers all the questions Today's designs require ever greater precision but design guides for specific digital interfaces are by nature conservative Now for the first time there's a complete guide to timing analysis and simulation that will help you manage the tradeoffs between signal integrity performance and cost Writing from the perspective of a practicing SI engineer and team lead Greg Edlund of IBM presents deep knowledge and quantitative techniques for making better decisions about digital interface design Edlund shares his insights into how and why digital interfaces fail revealing how fundamental sources of pathological effects can combine to create fault conditions You won't

just learn Edlund's expert techniques for avoiding failures you'll learn how to develop the right approach for your own projects and environment Coverage includes Systematically ensure that interfaces will operate with positive timing margin over the product's lifetime without incurring excess cost Understand essential chip to chip timing concepts in the context of signal integrity Collect the right information upfront so you can analyze new designs more effectively Review the circuits that store information in CMOS state machines and how they fail Learn how to time common clock source synchronous and high speed serial transfers Thoroughly understand how interconnect electrical characteristics affect timing propagation delay impedance profile crosstalk resonances and frequency dependent loss Model 3D discontinuities using electromagnetic field solvers Walk through four case studies coupled differential vias land grid array connector DDR2 memory data transfer and PCI Express channel Appendices present a refresher on SPICE modeling and a high level conceptual framework for electromagnetic field behavior Objective realistic and practical this is the signal integrity resource engineers have been searching for Preface xiii Acknowledgments xvi About the Author xix About the Cover xx Chapter 1 Engineering Reliable Digital Interfaces 1 Chapter 2 Chip to Chip Timing 13 Chapter 3 Inside IO Circuits 39 Chapter 4 Modeling 3D Discontinuities 73 Chapter 5 Practical 3D Examples 101 Chapter 6 DDR2 Case Study 133 Chapter 7 PCI Express Case Study 175 Appendix A A Short CMOS and SPICE Primer 209 Appendix B A Stroll Through 3D Fields 219 Endnotes 233 Index 235

Digital Communications Test and Measurement Dennis Derickson, Marcus Müller, 2007-12-10 A Comprehensive Guide to Physical Layer Test and Measurement of Digital Communication Links Today's new data communication and computer interconnection systems run at unprecedented speeds presenting new challenges not only in the design but also in troubleshooting test and measurement This book assembles contributions from practitioners at top test and measurement companies component manufacturers and universities It brings together information that has never been broadly accessible before information that was previously buried in application notes seminar and conference presentations short courses and unpublished works Readers will gain a thorough understanding of the inner workings of digital high speed systems and learn how the different aspects of such systems can be tested The editors and contributors cover key areas in test and measurement of transmitters digital waveform and jitter analysis and bit error ratio receivers sensitivity jitter tolerance and PLL CDR characterization and high speed channel characterization in time and frequency domain Extensive illustrations are provided throughout Coverage includes Signal integrity from a measurement point of view Digital waveform analysis using high bandwidth real time and sampling equivalent time oscilloscopes Bit error ratio measurements for both electrical and optical links Extensive coverage on the topic of jitter in high speed networks State of the art optical sampling techniques for analysis of 100 Gbit/s signals Receiver characterization clock recovery phase locked loops jitter tolerance and transfer functions sensitivity testing and stressed waveform receiver testing Channel and system characterization TDR T and frequency domain based alternatives Testing and measuring PC architecture communication links PCIexpress SATA and FB

DIMM A Signal Integrity Engineer's Companion Geoff Lawday, David Ireland, Greg Edlund, 2008-06-12 A Signal Integrity Engineer's Companion Real Time Test and Measurement and Design Simulation Geoff Lawday David Ireland Greg Edlund Foreword by Chris Edwards Editor IET Electronics Systems and Software magazine Prentice Hall Modern Semiconductor Design Series Prentice Hall Signal Integrity Library Use Real World Test and Measurement Techniques to Systematically Eliminate Signal Integrity Problems This is the industry's most comprehensive authoritative and practical guide to modern Signal Integrity SI test and measurement for high speed digital designs Three of the field's leading experts guide you through systematically detecting observing analyzing and rectifying both modern logic signal defects and embedded system malfunctions The authors cover the entire life cycle of embedded system design from specification and simulation onward illuminating key techniques and concepts with easy to understand illustrations Writing for all electrical engineers signal integrity engineers and chip designers the authors show how to use real time test and measurement to address today's increasingly difficult interoperability and compliance requirements They also present detailed start to finish case studies that walk you through commonly encountered design challenges including ensuring that interfaces consistently operate with positive timing margins without incurring excessive cost calculating total jitter budgets and managing complex tradeoffs in high speed serial interface design Coverage includes Understanding the complex signal integrity issues that arise in today's high speed designs Learning how eye diagrams automated compliance tests and signal analysis measurements can help you identify and solve SI problems Reviewing the electrical characteristics of today's most widely used CMOS IO circuits Performing signal path analyses based on intuitive Time Domain Reflectometry TDR techniques Achieving more accurate real time signal measurements and avoiding probe problems and artifacts Utilizing digital oscilloscopes and logic analyzers to make accurate measurements in high frequency environments Simulating real world signals that stress digital circuits and expose SI faults Accurately measuring jitter and other RF parameters in wireless applications About the Authors Dr Geoff Lawday is Tektronix Professor in Measurement at Buckinghamshire New University England He delivers courses in signal integrity engineering and high performance bus systems at the University Tektronix laboratory and presents signal integrity seminars throughout Europe on behalf of Tektronix David Ireland European and Asian design and manufacturing marketing manager for Tektronix has more than 30 years of experience in test and measurement He writes regularly on signal integrity for leading technical journals Greg Edlund Senior Engineer IBM Global Engineering Solutions division has participated in development and testing for ten high performance computing platforms He authored Timing Analysis and Simulation for Signal Integrity Engineers Prentice Hall

Advances in Mechatronics, Robotics and Automation II Prasad Yarlagadda, 2014-04-04 Selected peer reviewed papers from the 2014 2nd International Conference on Mechatronics Robotics and Automation ICMRA 2014 March 8 9 2014 Zhuhai China

ASIC and FPGA Verification Richard Munden, 2004-10-23 Richard Munden demonstrates how to create and use simulation models for verifying ASIC and FPGA

designs and board level designs that use off the shelf digital components Based on the VHDL VITAL standard these models include timing constraints and propagation delays that are required for accurate verification of today s digital designs ASIC and FPGA Verification A Guide to Component Modeling expertly illustrates how ASICs and FPGAs can be verified in the larger context of a board or a system It is a valuable resource for any designer who simulates multi chip digital designs Provides numerous models and a clearly defined methodology for performing board level simulation Covers the details of modeling for verification of both logic and timing First book to collect and teach techniques for using VHDL to model off the shelf or IP digital components for use in FPGA and board level design verification Engineering the Complex SOC Chris Rowen,2008-11-11 Engineering the Complex SOC The first unified hardware software guide to processor centric SOC design Processor centric approaches enable SOC designers to complete far larger projects in far less time Engineering the Complex SOC is a comprehensive example driven guide to creating designs with configurable extensible processors Drawing upon Tensilica s Xtensa architecture and TIE language Dr Chris Rowen systematically illuminates the issues opportunities and challenges of processor centric design Rowen introduces a radically new design methodology then covers its essential techniques processor configuration extension hardware software co generation multiple processor partitioning communication and more Coverage includes Why extensible processors are necessary shortcomings of current design methods Comparing extensible processors to traditional processors and hardwired logic Extensible processor architecture and mechanisms of processor extensibility Latency throughput coordination of parallel functions hardware interconnect options management of design complexity and other issues Multiple processor SOC architecture for embedded systems Task design from the viewpoints of software and hardware developers Advanced techniques implementing complex state machines task to task synchronization power optimization and more Toward a sea of processors Long term trends in SOC design and semiconductor technology For all architects hardware engineers software designers and SOC program managers involved with complex SOC design and for all managers investing in SOC designs platforms processors or expertise PRENTICE HALL Professional Technical Reference Upper Saddle River NJ 07458 www.phptr com Computers as Components Wayne Hendrix Wolf,2005 This work unravels the complexity of embedded systems e g cell phones microwaves and information appliances and of the process tools and techniques necessary for designing them Practical FPGA Programming in C David Pellerin, Scott Thibault,2005 FPGA brings high performance applications to market quickly this book covers the many emerging platforms in a proven effective manner **Readings in Hardware/Software Co-Design** Giovanni De Micheli, Rolf Ernst, Wayne Wolf,2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s Embedded Systems Design with 8051 Microcontrollers Zdravko Karakehayov,2018-10-08 A presentation of developments in microcontroller technology providing lucid instructions on its many and varied applications It focuses on the popular eight bit microcontroller the 8051 and the

83C552 The text outlines a systematic methodology for small scale control dominated embedded systems and is accompanied by a disk of all the example problems included in the book **Hardware/Software Co-Design** Jørgen Staunstrup, Wayne Wolf, 2013-04-17 Introduction to Hardware Software Co Design presents a number of issues of fundamental importance for the design of integrated hardware software products such as embedded communication and multimedia systems This book is a comprehensive introduction to the fundamentals of hardware software co design Co design is still a new field but one which has substantially matured over the past few years This book written by leading international experts covers all the major topics including fundamental issues in co design hardware software co synthesis algorithms prototyping and emulation target architectures compiler techniques specification and verification system level specification Special chapters describe in detail several leading edge co design systems including Cosyma LYCOS and Cosmos Introduction to Hardware Software Co Design contains sufficient material for use by teachers and students in an advanced course of hardware software co design It also contains extensive explanation of the fundamental concepts of the subject and the necessary background to bring practitioners up to date on this increasingly important topic

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