```
// Test Plan - Verify: (1) Power-up reset, (2) match ASMD chart in Fig. 8-9 (d).
// (3) recover from reset on-the-fly

module t_Prob_8_9;
  wire E, F;
  wire [3: 0] A;
  wire A2, A3;
  reg Start, clock, reset_b;

  Prob_8_9 M0 (E, F, A, A2, A3, Start, clock, reset_b);

  initial #500 $finish;
  initial begin clock = 0; forever #5 clock = ~clock; end
  initial begin reset_b = 0; #2 reset_b = 1; end
  initial fork
    #20 Start = 1;
    #40 reset_b = 0;
    #62 reset_b = 1;
  join
endmodule
```
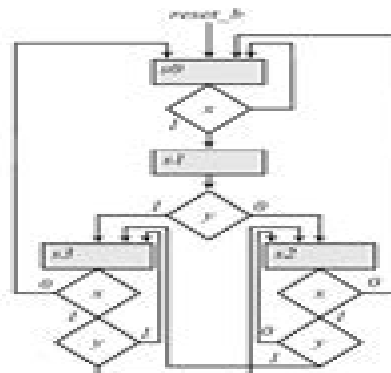
8.10


```
module Prob_8_10 (input x, y, clock, reset_b);
  reg [ 1: 0]    state, next_state;
  parameter    s0 = 2'b00, s1 = 2'b01, s2 = 2'b10, s3 = 2'b11;
  always @ (posedge clock, negedge reset_b)
    if (reset_b == 0) state <= s0; else state <= next_state;

  always @ (state, x, y) begin
    next_state = s0;
    case (state)
      s0: if (x == 0) next_state = s0; else next_state = s1;
      s1: if (y == 0) next_state = s2; else next_state = s3;
      s2: if (x == 0) next_state = s0; else if (y == 0) next_state = s2; else next_state = s3;
      s3: if (x == 0) next_state = s0; else if (y == 0) next_state = s2; else next_state = s3;
    endcase
  end
endmodule
```

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engineers regarding the current status of nanocomputing material and the reliability of systems built from such miniscule devices are difficult to articulate and answer We have found a lack of resources in the confines of a single volume that at least partially attempts to answer these questions We believe that this volume contains a large amount of research material as well as new ideas that will be very useful for some one starting research in the arena of nanocomputing not at the device level but the problems one would face at system level design and validation when nanoscopic physicality will be present at the device level   *Computer System Architecture* M. Morris Mano,1982 Focused primarily on hardware design and organization and the impact of software on the architecture this volume first covers the basic organization design and programming of a simple digital computer then explores the separate functional units in detail FEATURES develops an elementary computer to demonstrate by example the organization and design of digital computers uses a simple register transfer language to specify various computer operations

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